Many ways to shrink: The right moves to 10 nanometer and beyond

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President & Chief Technology Officer

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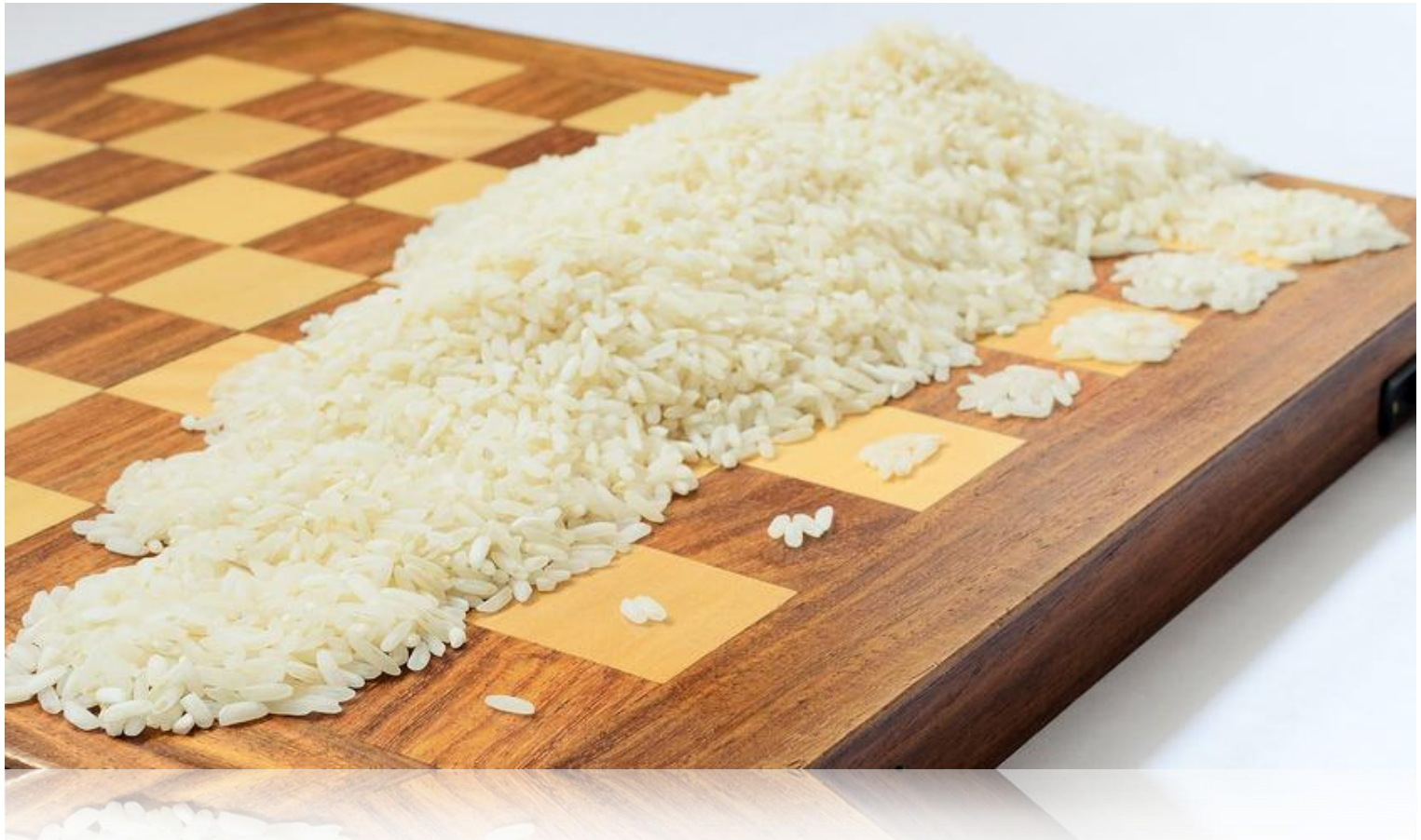
INVESTOR DAY
ASMLSMALLTALK2014
LONDON

Content

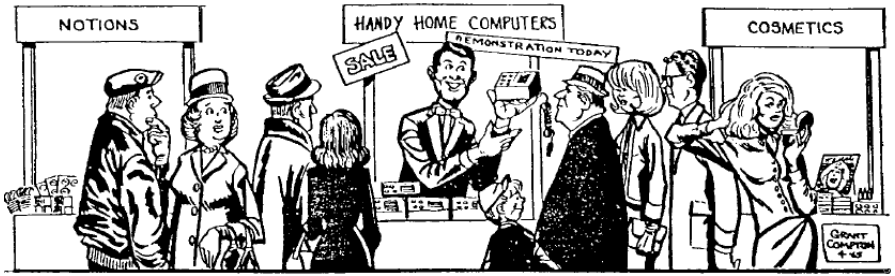
- Industry Challenges
  - The desire to shrink
  - The device challenges
  - The scaling challenges
- ASML Solutions
  - Our holistic approach to extend immersion
  - The process simplification by using EUV

Moore’s Law: the rice-and-chessboard challenge

The benefits of shrink are irresistible



Driving the semiconductor industry: Moore's Law;
"…home computers…and personal portable communication…"



Gordon Moore's prediction, 1965

Integrated circuits will lead to such wonders as home computers—or at least terminals connected to a central computer—automatic controls for automobiles, and personal portable communications equipment. The electronic wristwatch needs only a display to be feasible today.

But the biggest potential lies in the production of large systems. In telephone communications, integrated circuits in digital filters will separate channels on multiplex equipment. Integrated circuits will also switch telephone circuits and perform data processing.

Reality, ~ 50 years later, 2014

Source: Gordon E. Moore,
"Cramming More Components onto Electronic Circuits",
Electronics, pp114-117, April 19, 1965

Some question if Moore's Law can continue

cnet
Search CNET
End of Moore's Law: It's not
about physics
A DARPA director argues that the end of the Moore's Law -- which
why you now have a tablet in your hand -- could come about bec
insurmountable economic challenges.
by Brooke Crothers @mbrookec / August 28, 2013 6:15 AM PDT

ZDNet
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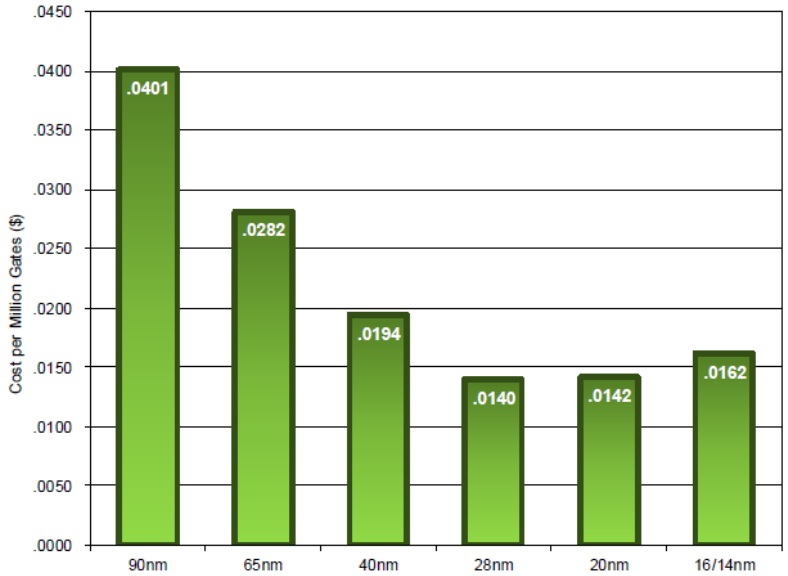
Moore's Law: the end is near-ish!

PCWorld
Work. Life. Productivity.

Seeking Alpha α
Read. Decide. Invest.
Intel: The End Of Moore's L
OK, OK, so we are not yet at the end of Moo
end from here.
Moore's Law comes to us from Gordon Moore
Semiconductor (FCS) and, later, Intel Corpor
Moore wrote a paper in 1965 describing his
transistors on a given cost integrated circui
invention of the integrated circuit, and his
transistors would continue to double, at th
the foreseeable future. The subtle detail th
discussions of Moore's Law is that the num
SAME COST. So the size of a transistor has
less expensive.

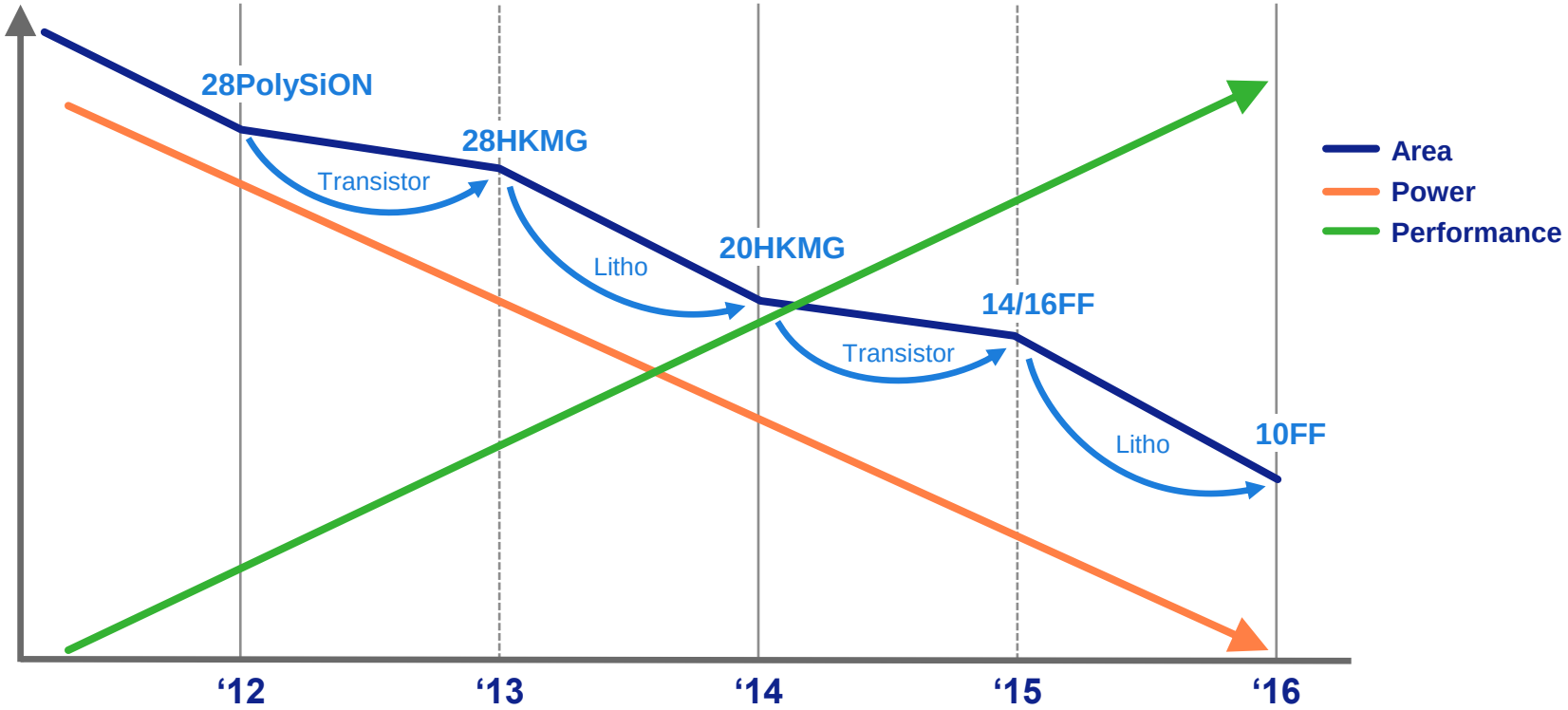
IBS



S
Node of Moore's
nc.
e imminent demise of Moore's Law
e predictions have been targeting
nd-point. But we need to
ctually the last node of Moore's

Mobile applications continue to be on an yearly cadence

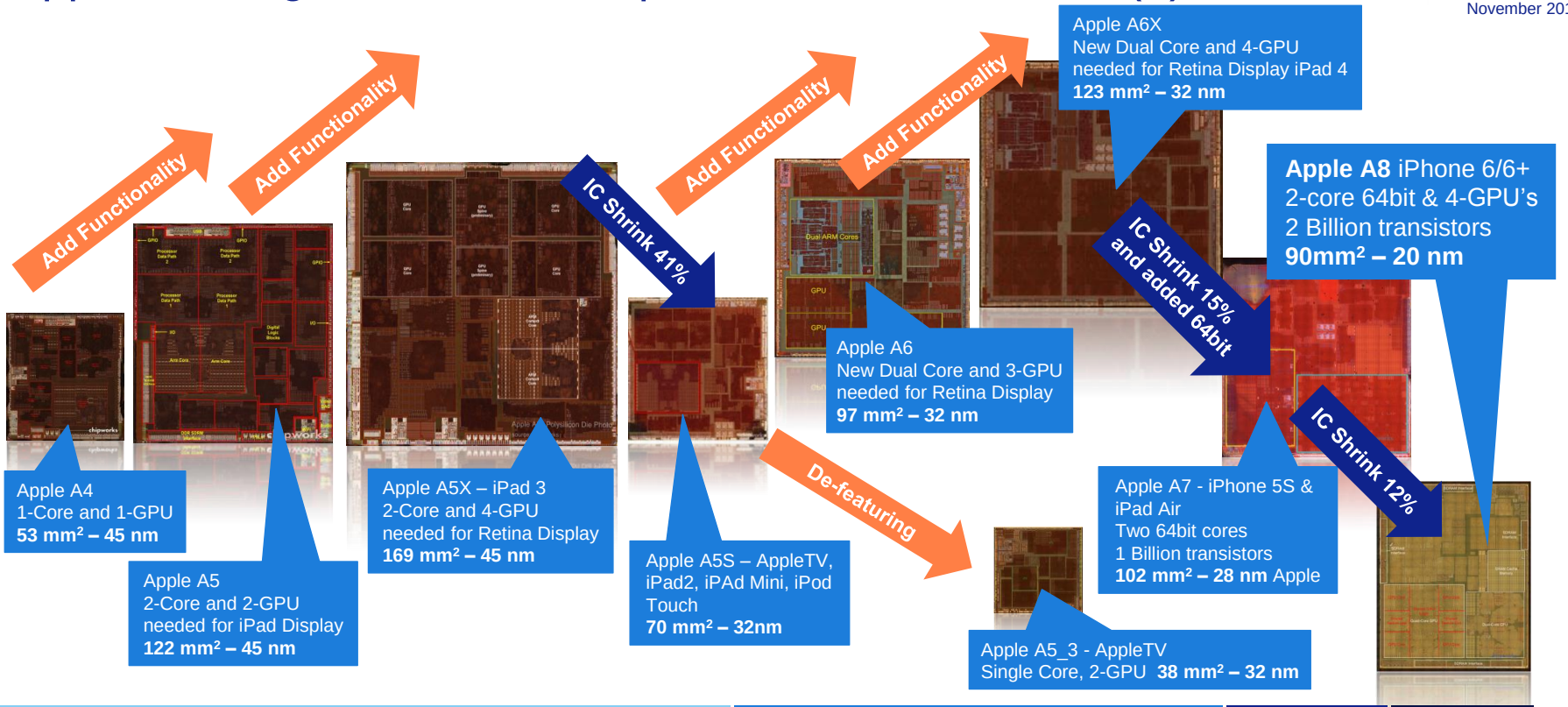
device and litho innovations driving area, power and performance



Source: Esin Terzioglu, Qualcomm, EUV symposium, Oct 2014

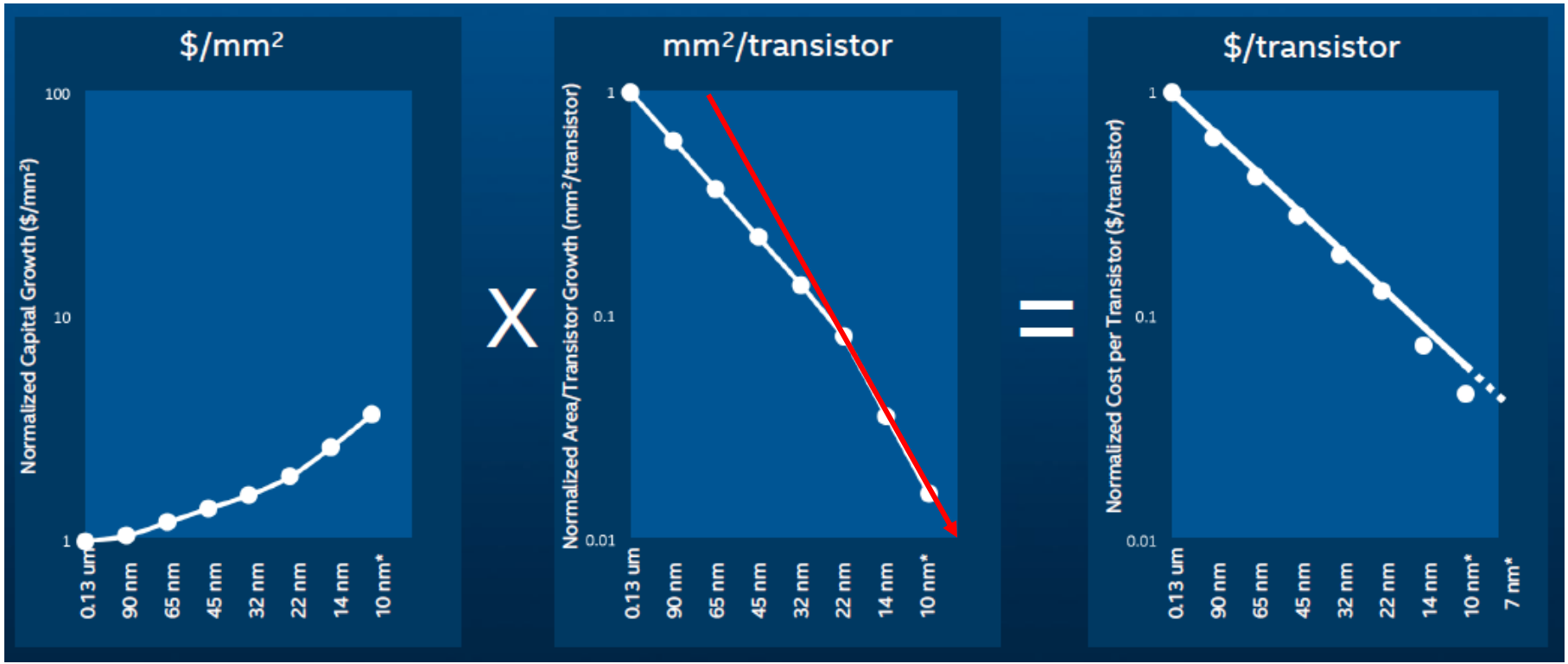
Mobile chips integrating functionality faster than shrink

Apple: first high volume 20nm process in the iPhone 6(+)



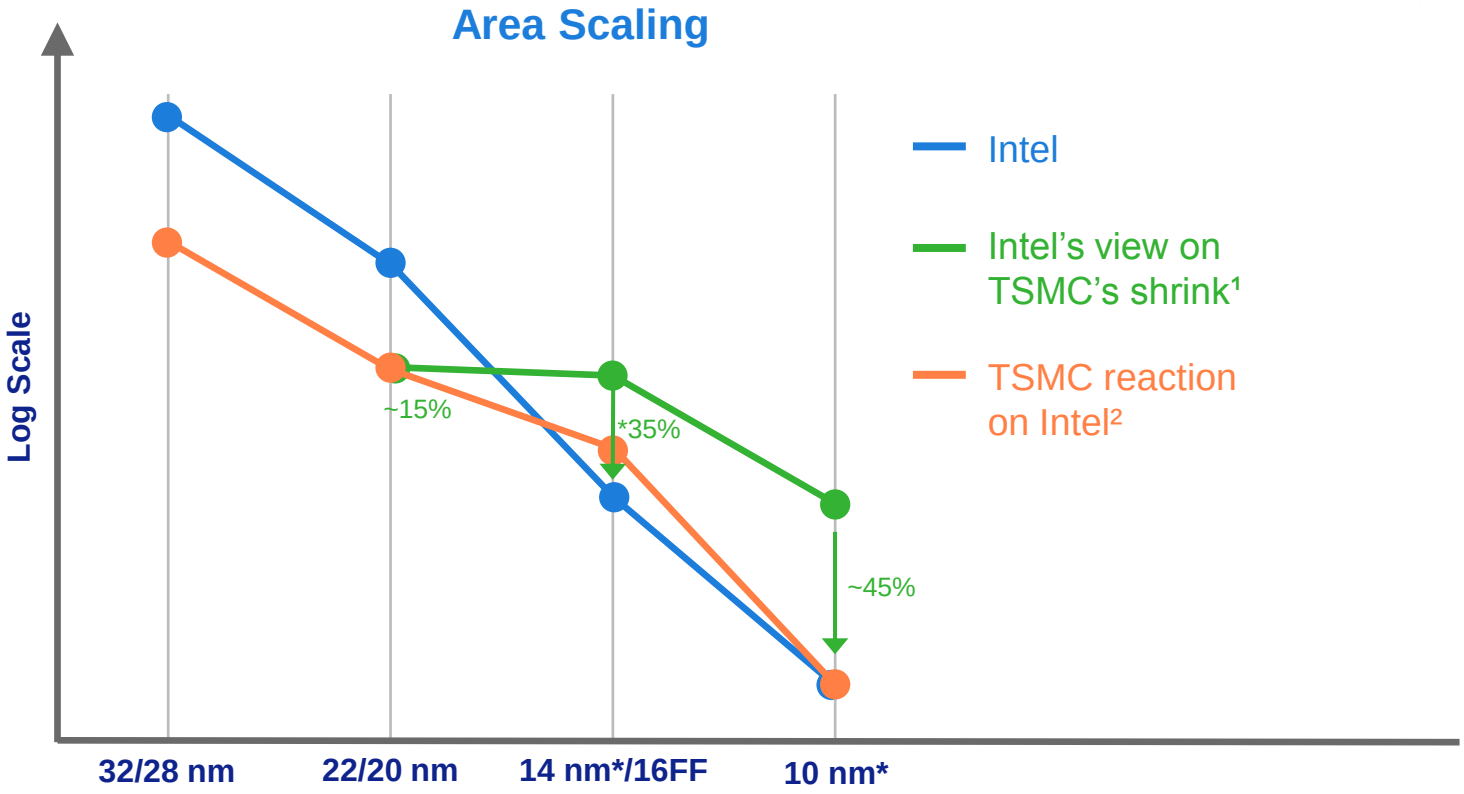
Source: Apple

And area and cost per function reduction accelerates



Source: Bill Holt, Intel, “Intel Investor meeting”, Nov 2014, *forecast

And is a competitive item between chip makers



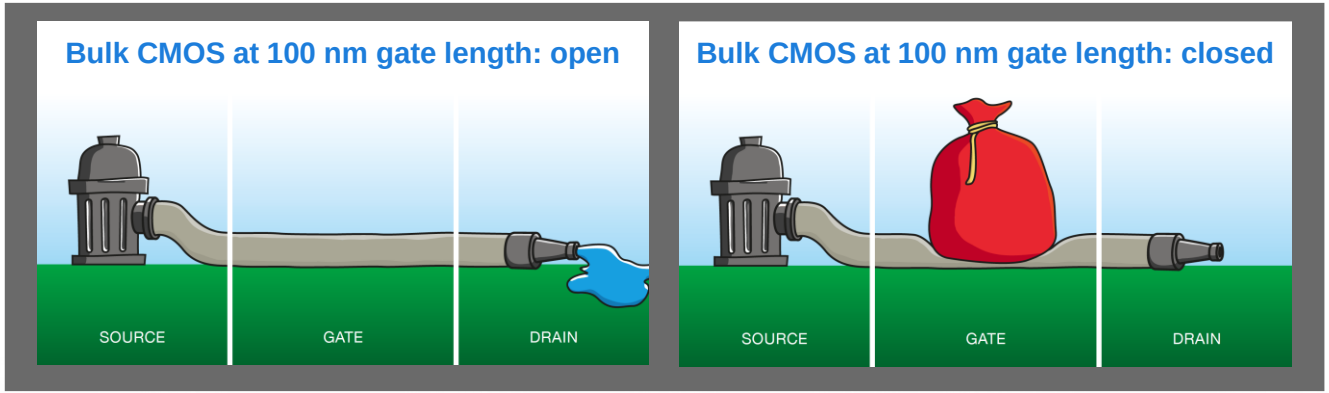
Sourcews: [1]Bill Holt, Intel investor conference, Nov 2013
[2]Mark Liu, TSMC analyst call, Jan 2014

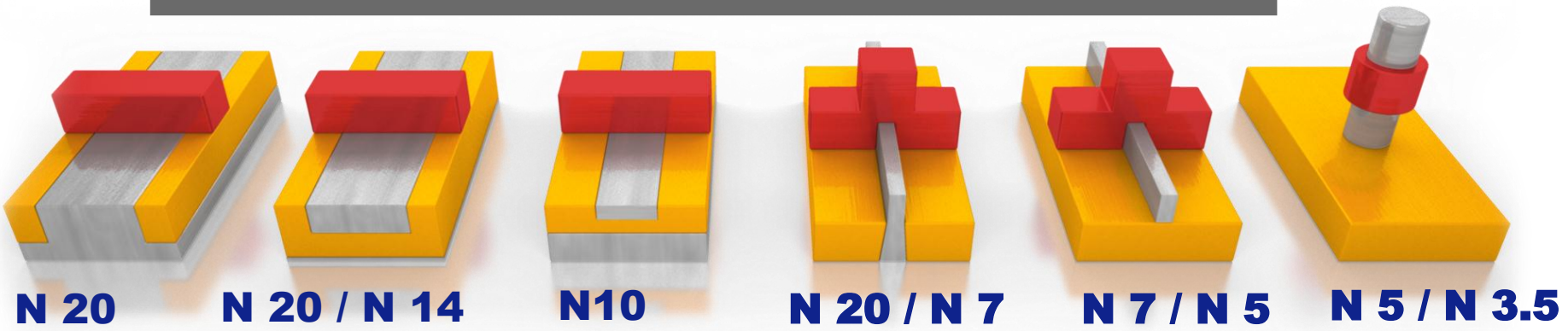
The challenge of Moore's law chessboard in numbers

What about our customers challenges?

1	2	4	8	16	32	64	128
256	512	1024	2048	4096	8192	16384	32768
65536	131072	262144	524288	1048576	2097152	4194304	8388608
16777216	33554432	67108864	1.34E+08	2.68E+08	5.37E+08	1.07E+09	2.15E+09
4.29E+09	8.59E+09	1.72E+10	3.44E+10	6.87E+10	1.37E+11	2.75E+11	5.5E+11
1.1E+12	2.2E+12	4.4E+12	8.8E+12	1.76E+13	3.52E+13	7.04E+13	1.41E+14
2.81E+14	5.63E+14	1.13E+15	2.25E+15	4.5E+15	9.01E+15	1.8E+16	3.6E+16
7.21E+16	1.44E+17	2.88E+17	5.76E+17	1.15E+18	2.31E+18	4.61E+18	9.22E+18

Shrink scenarios for logic devices





N 20

Bulk CMOS: Complementary Metal Oxide Semiconductor

N 20 / N 14

SOI: Partially depleted Silicon on insulator

N10

SOI: Fully depleted Silicon on insulator

N 20 / N 7

Bulk FinFet : fin field effect transistor

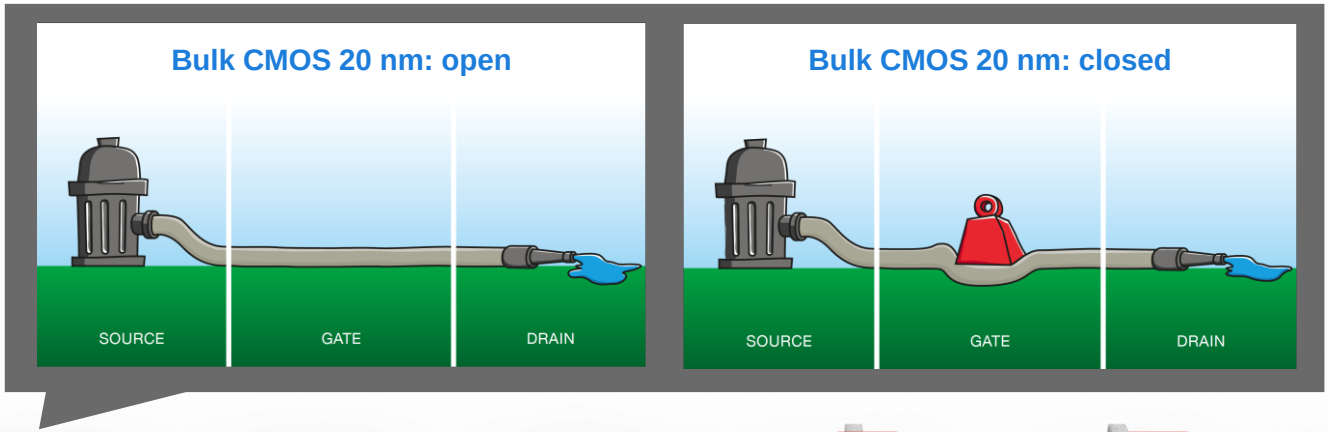
N 7 / N 5

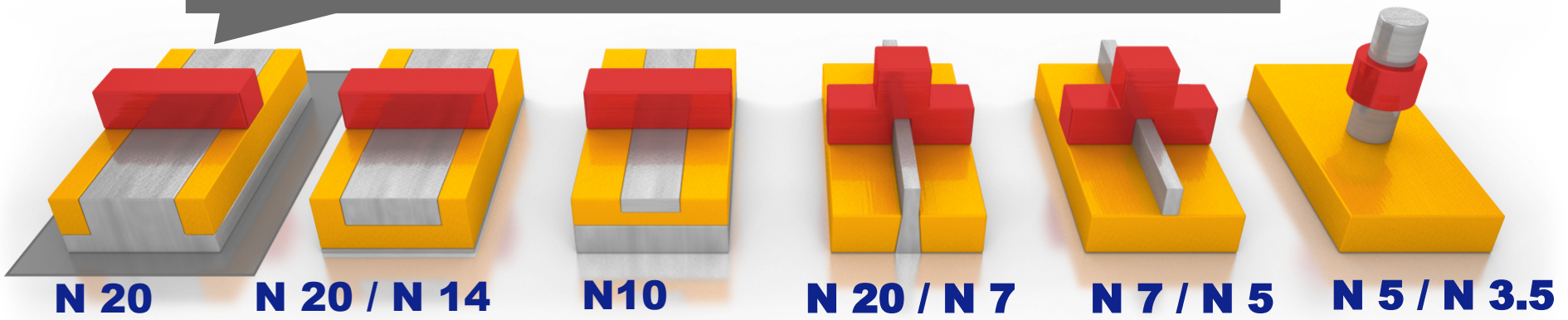
SOI FinFet : silicon on insulator fin field effect transistor, III-V

N 5 / N 3.5

Gate-all-around transistor

Shrink scenarios for logic devices





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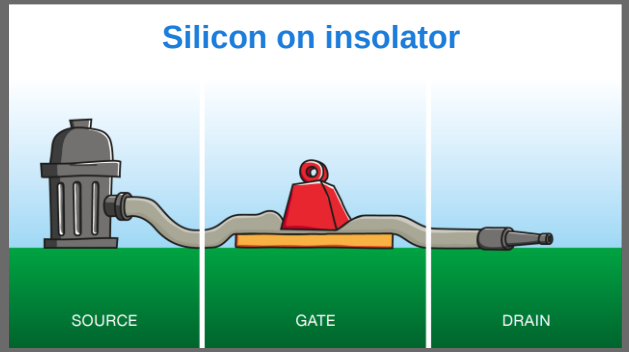
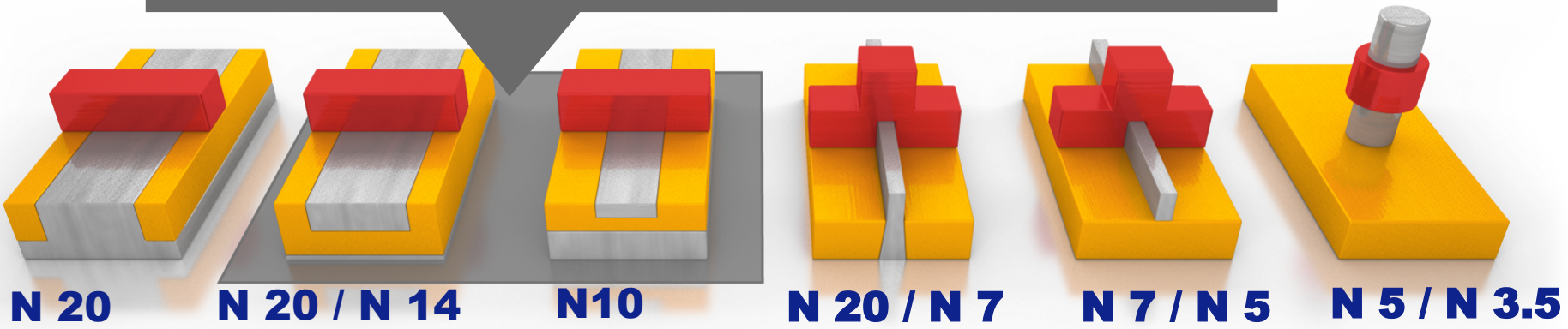
Solution 1:





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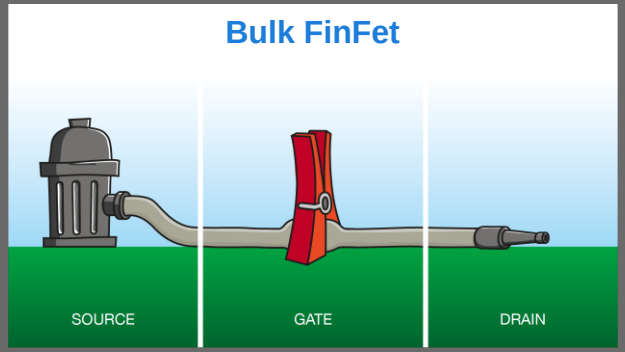
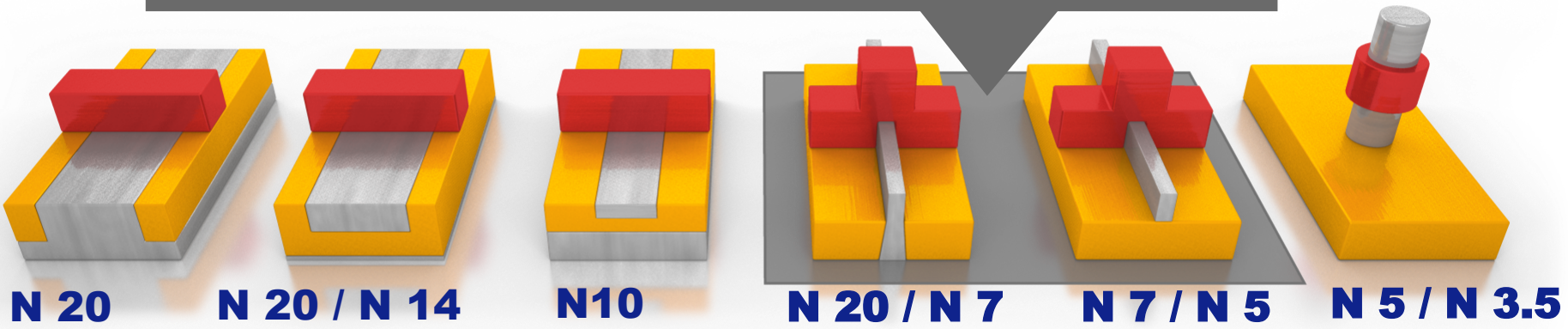
Shrink scenarios for logic devices

Solution 2:





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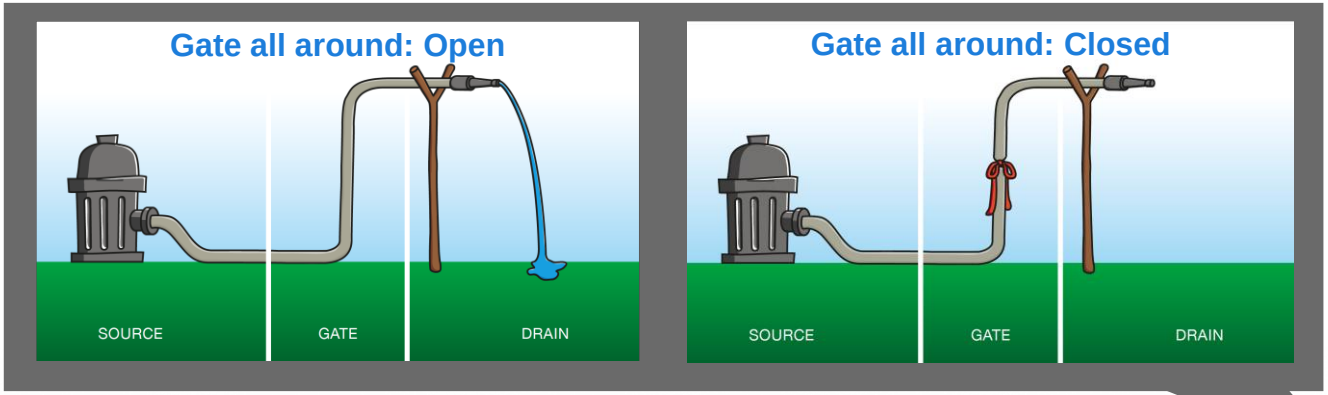

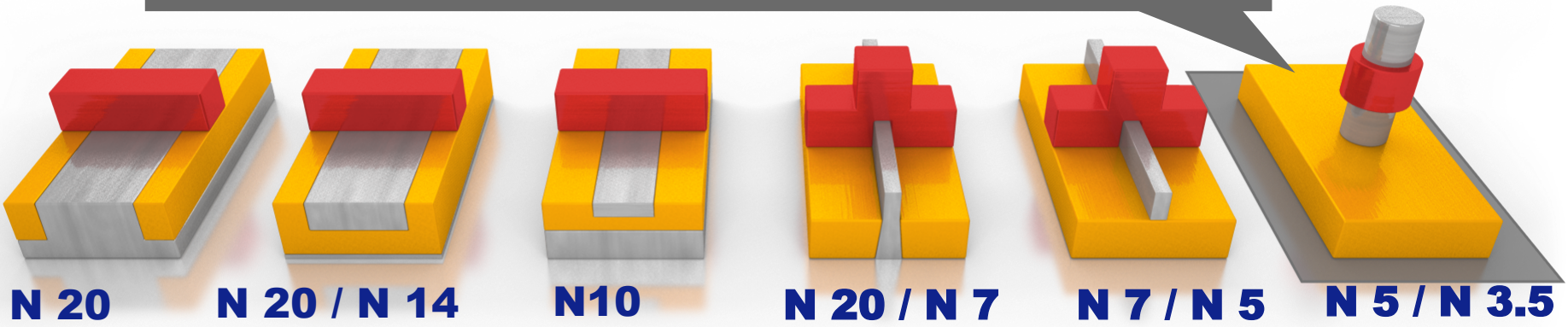

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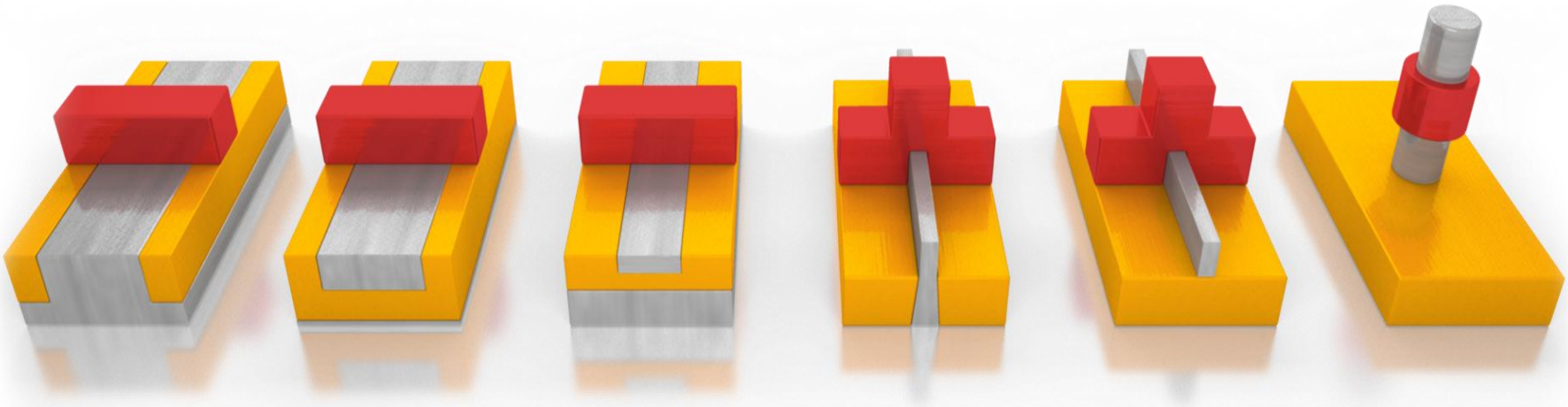
Gate-all-around transistor

No end in sight for logic scaling



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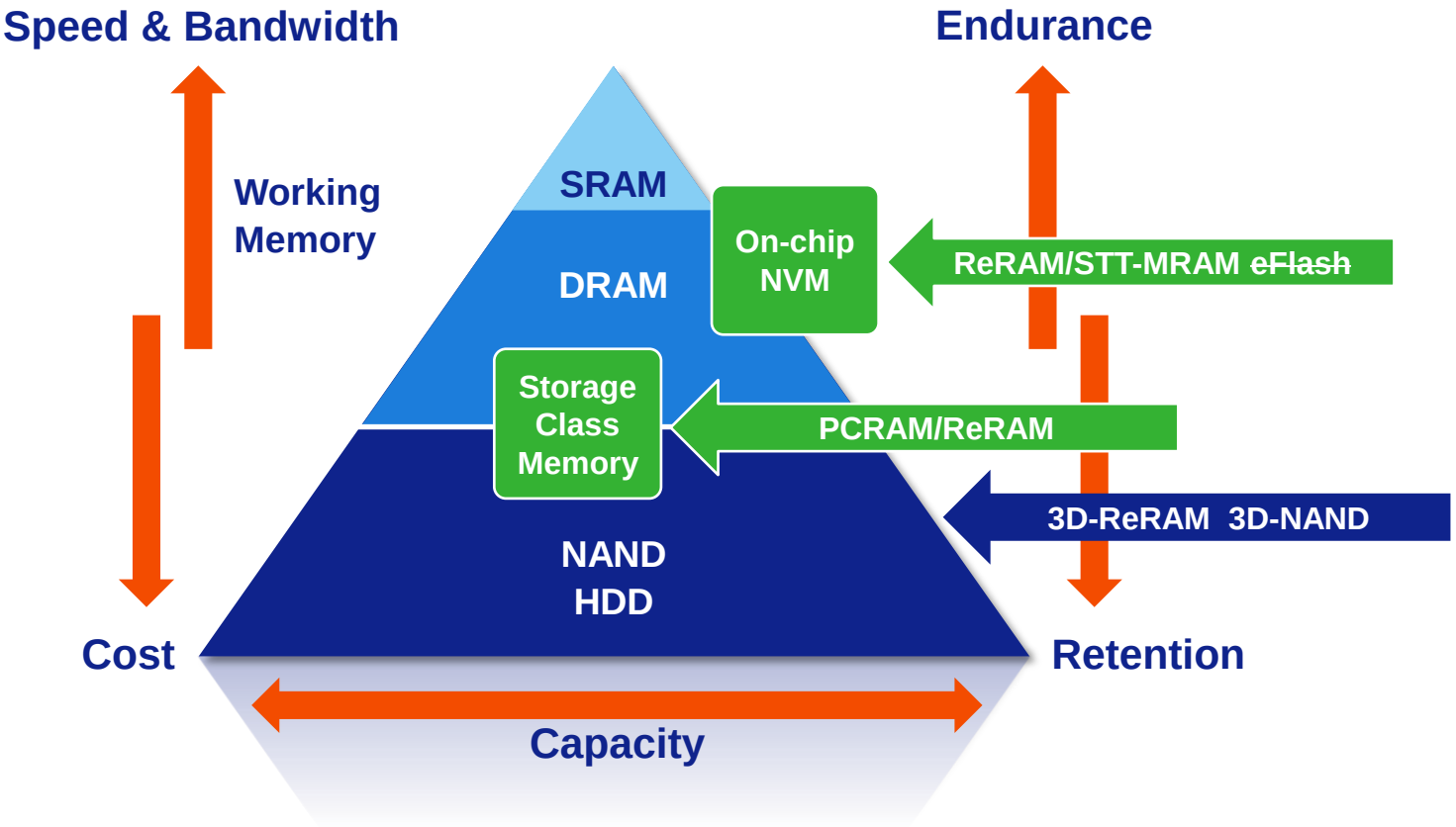
Gate-all-around transistor

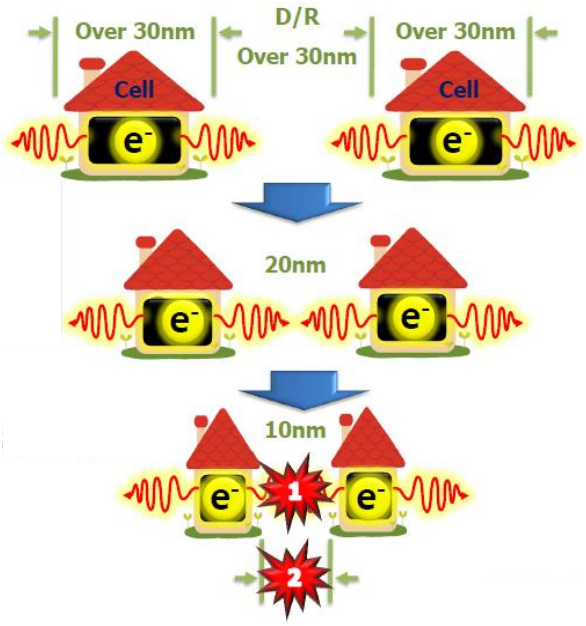
Significant architectural innovations ahead for Memory



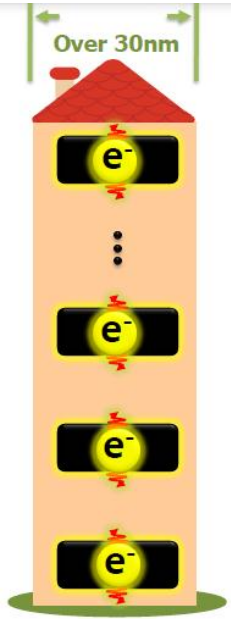
Source: Meng-Fan Chang, NTU Taiwan, Resistive memory workshop, Stanford, Oct 2014

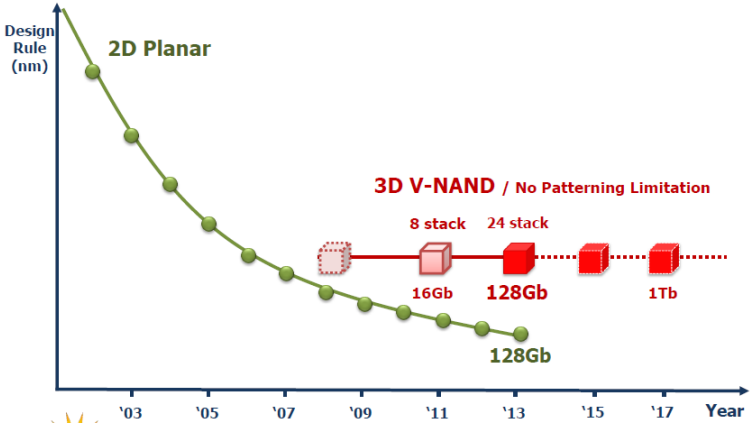
2D NAND vs 3D V-NAND Challenges

2D
Cell to cell interference



3D
Aspect ratio



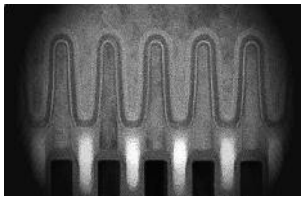


Source: Jung, Samsung, Flash Memory Summit, Santa Clara, Aug 2013

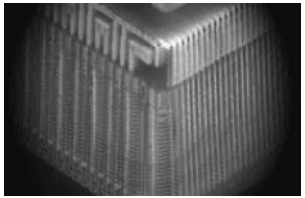
NAND memory continuing on multiple fronts

2D extensions, 3D introduction and ReRam coming

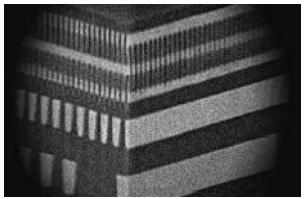
2D NAND

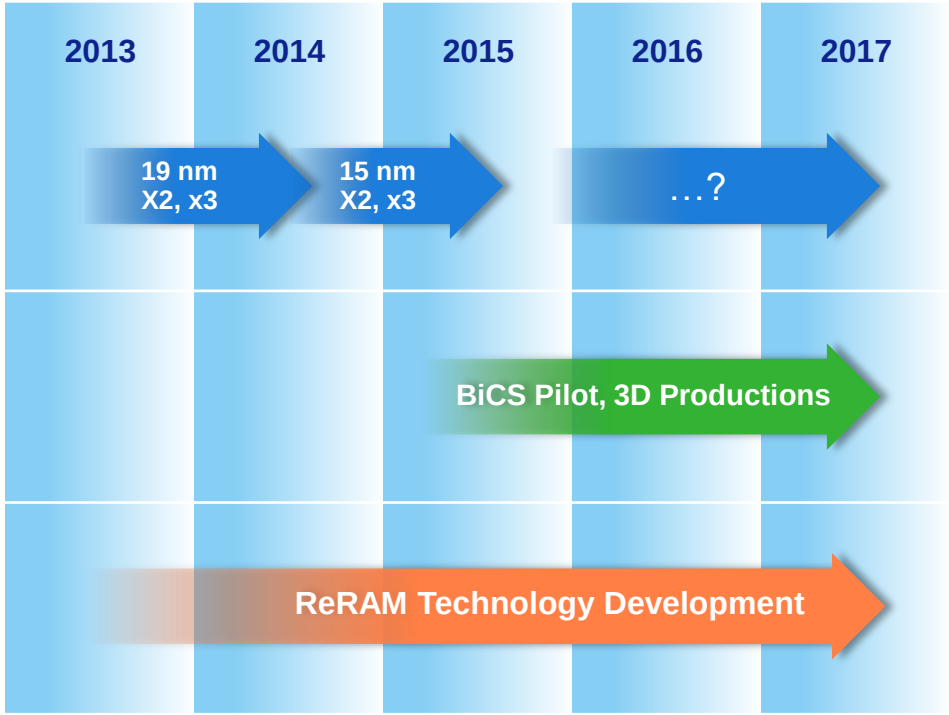


BiCS Bit
Cost
Scalable 3D
NAND



3D ReRAM
3D Resistive
RAM



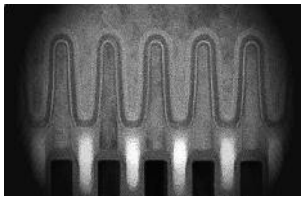


Source: Siva Sivaram, Sandisk investor day presentation, May 2014.

NAND memory continuing on multiple fronts

2D extensions, 3D introduction and ReRam coming

2D NAND



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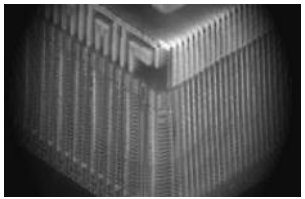

3D ReRAM
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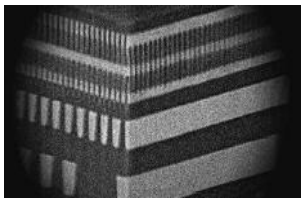
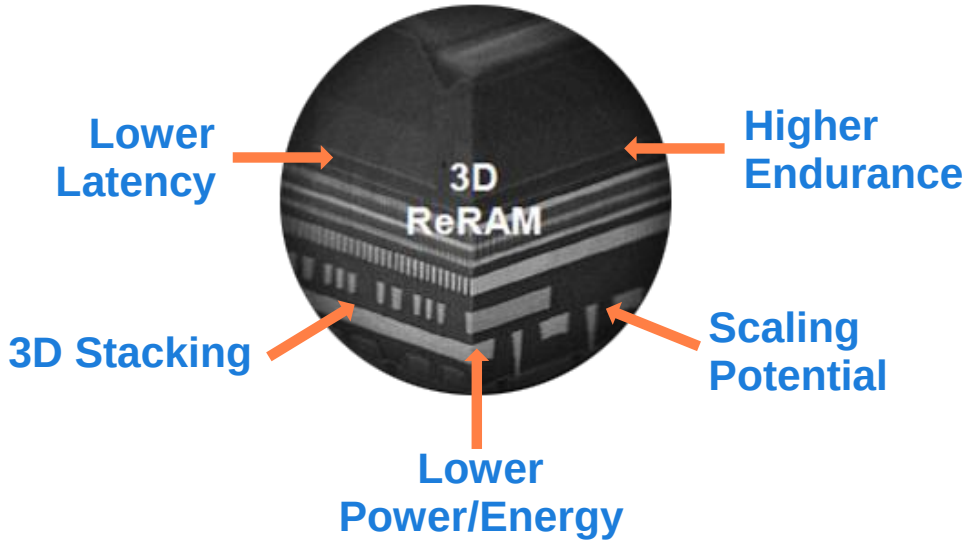


Scalable Below 10 nm;
New Product Categories



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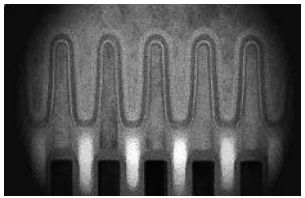
2D NAND



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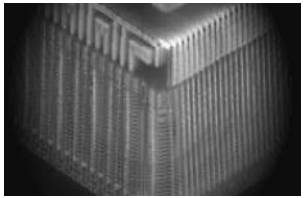
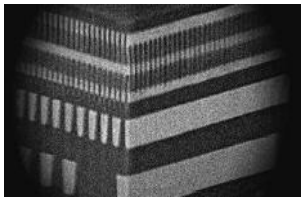
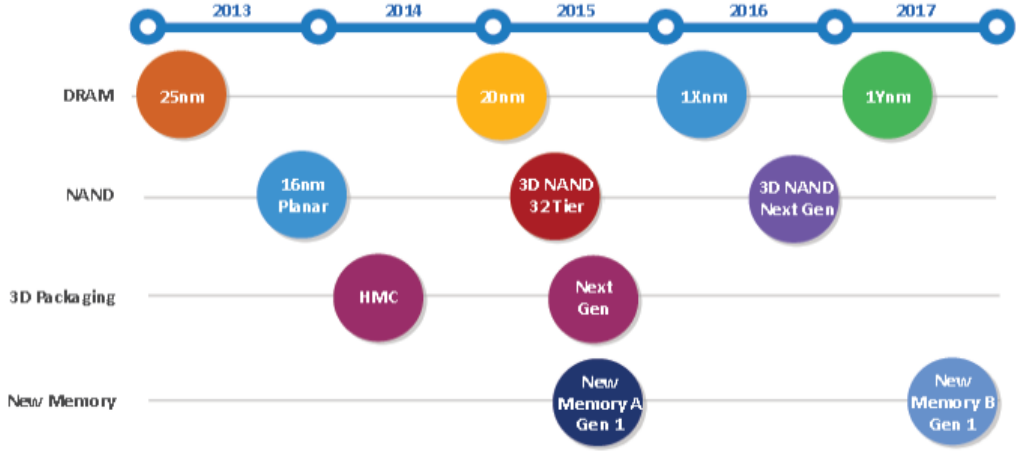
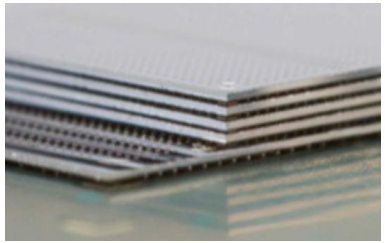


3D ReRAM
3D Resistive
RAM

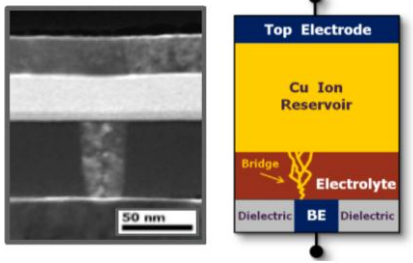


Memory Technology Timelines





Hybrid Memory Cube



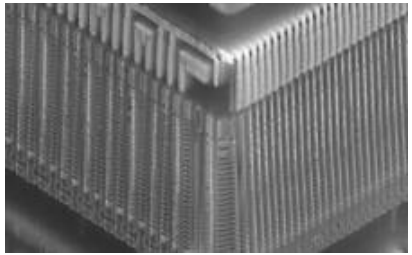
Resistive RAM

Source: Siva Sivaram, Sandisk investor day, May 2014
Scott DeBoer, Micron investor day, Aug 2014

Critical requirements for scaling 3D memory devices

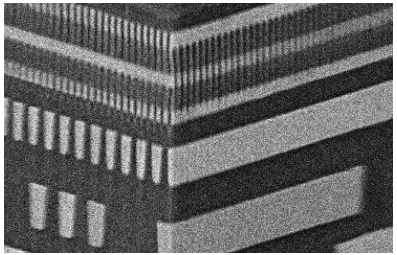
Etch aspect ratio vs litho scaling cost challenge

Vertical NAND



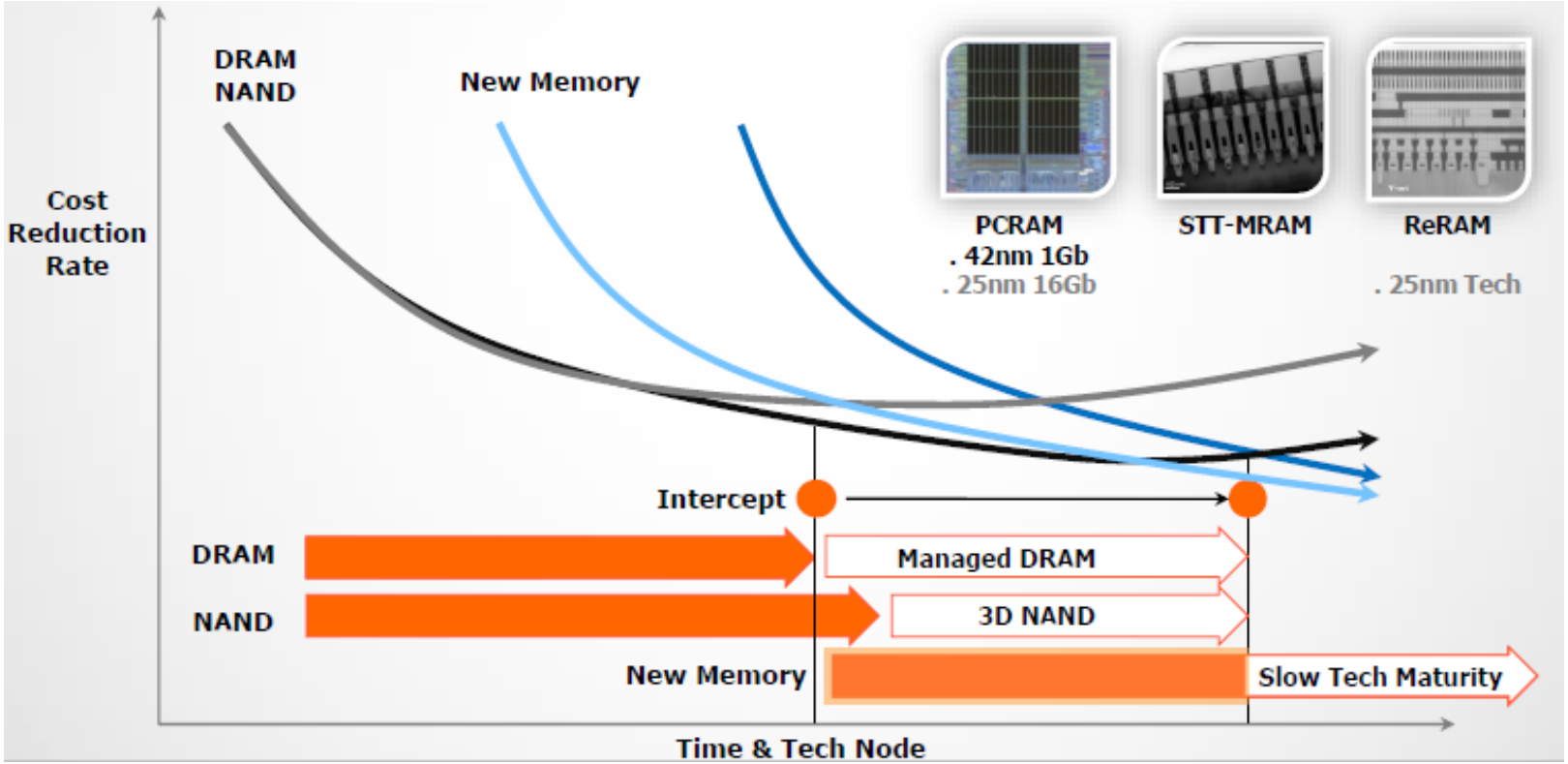
- Gates around conductive vertical channel
- Lithography light, critical overlay to top layer
- Deposition and deep etch intensive, horizontal density limited due to etch aspect ratio. Key : deep contact etch
- Large gate size

Cross bar ReRAM



- Perpendicular gate and channel architecture with horizontal conduction
- Lithography intensive (< 15nm, EUV)
- Deposition and litho etch per layer similar to 2D, density determined by litho
- Scalable gate possible

New memory competes with DRAM and NAND extensions and its likely delayed transition determined by cost scaling



Source: S.W. Park, Hynix, ITPC Hawaii, Nov 2014

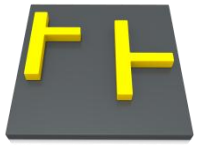
Sub-resolution imaging requires multiple litho steps

Process Flow

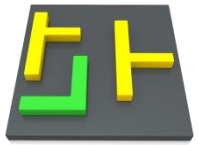
2D Multi Patterning or EUV single expose

LELE (or EUV SE)

LE #1



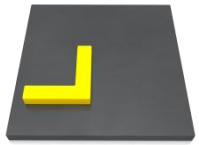
LE #2



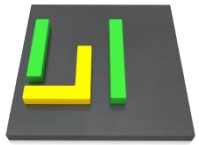
- Suitable for 1D or 2D patterning
- Overlay control of each layer is a key

LELELE (or EUV SE)

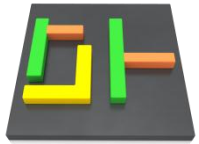
LE #1



LE #2



LE #3



1D Self Aligned Multiple Patterning (SAMP)

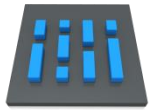
SADP (D=Double)

Mandrel

Spacer

Spacer cut

Patterning cut(s)

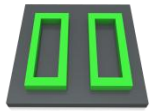


- Suitable for 1D layout (← better CD, LWR control)
- May need multiple cut patterns

SAQP (Q=Quadruple)

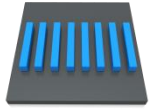
Mandrel

Spacer #1

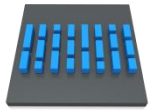


Spacer #2

Spacer cut

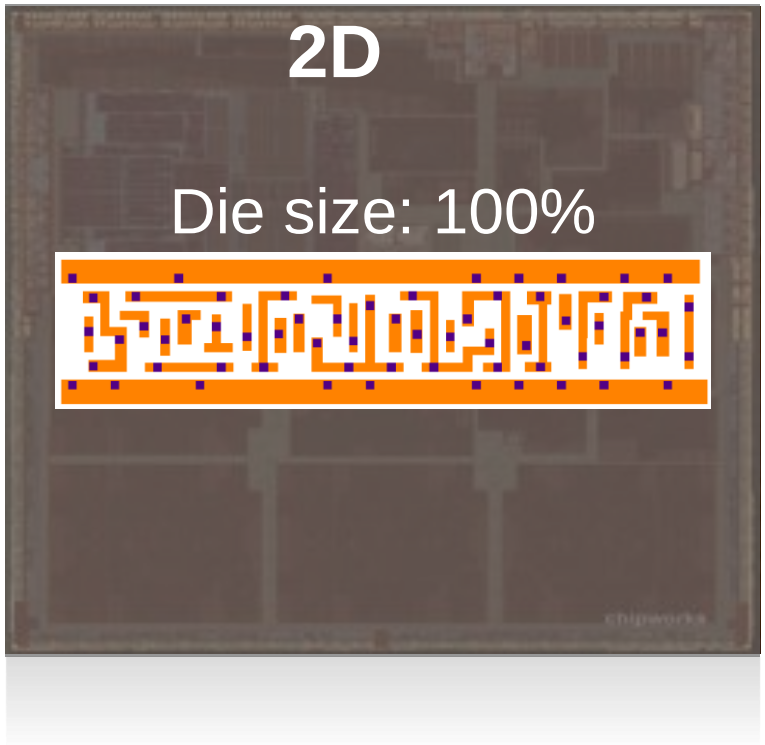


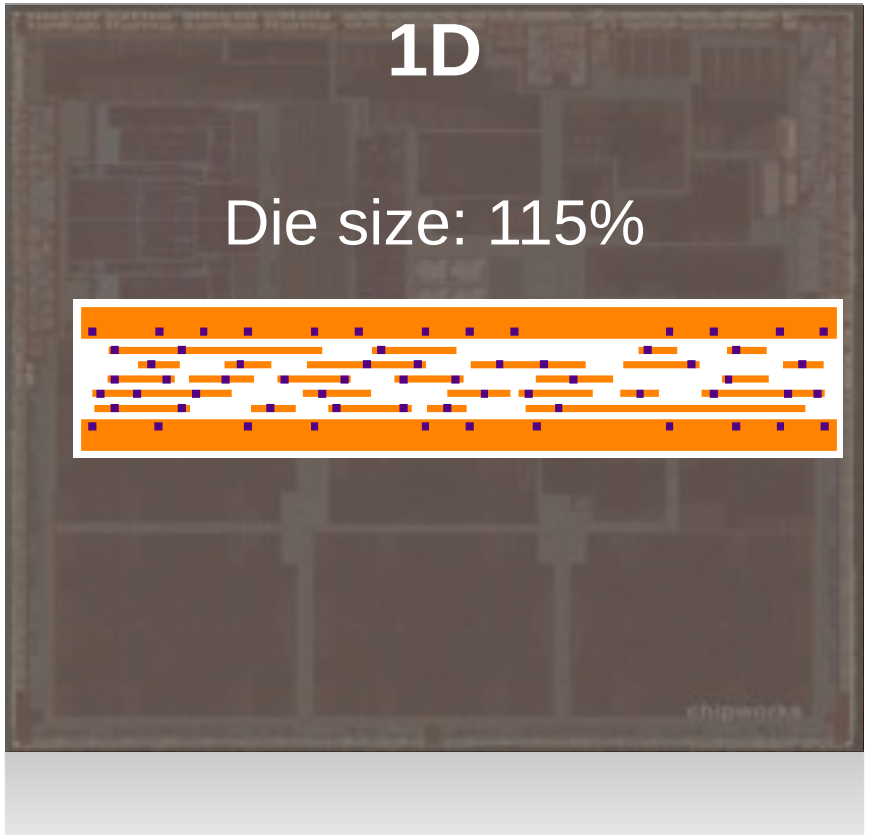
Patterning cut(s)



10nm logic design can be done in 1D

..but at the penalty of 15% larger die at comparable design rules





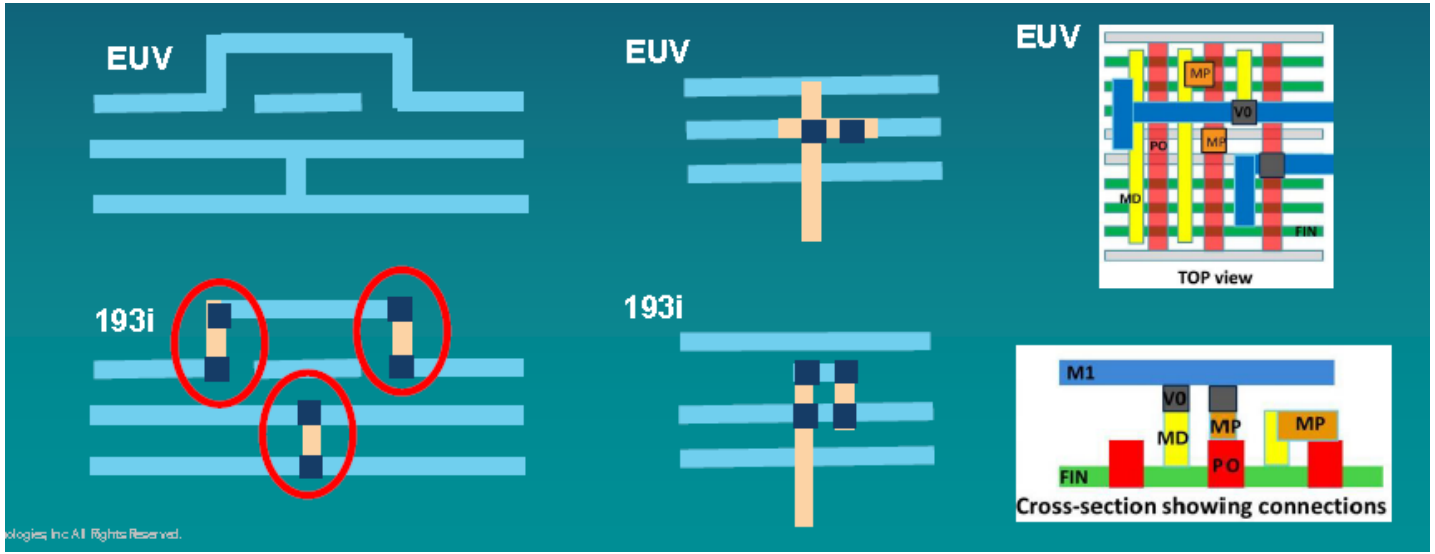
EUV: reduced complexity & design rule simplification

Allowing 2D structures and potentially better yield

Able to employ jogs
Reduced # vias (better yield)
Less min. length (area) wires
Able to connect to neighbor wire

Better freedom
for redundant via
insertion

Reduced MOL
complexity
by 2D M1



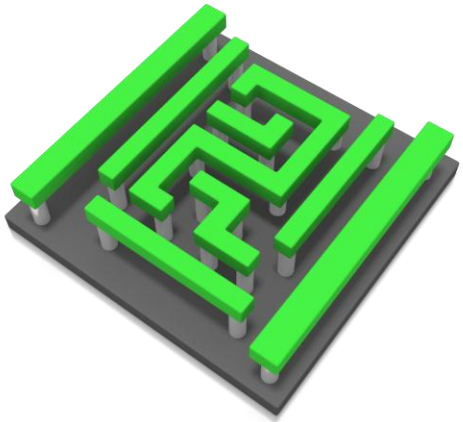
See
next
slide

Source: Esin Terzioglu, Qualcomm, EUV symposium, Oct 2014

10nm patterning choices & cost estimates

EUV lowest cost and complexity for 2D structures

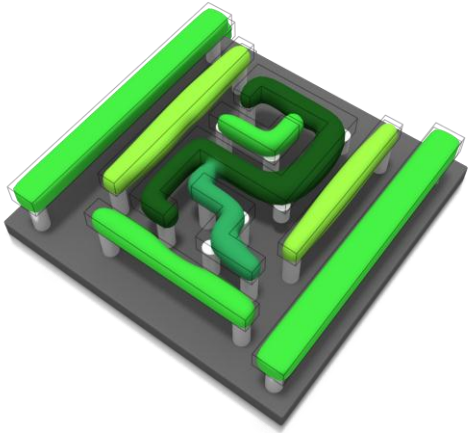
EUV
2D structure
Single layer solution



Cost for 1 layer 100%

Good pattern fidelity
Re-use existing designs

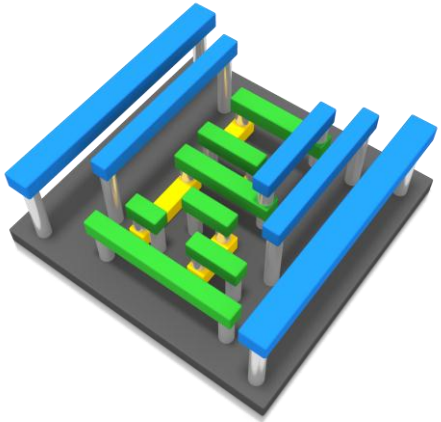
ArFi LE^4
2D structure
Single layer solution



Cost for 1 layer ~ 170%

Insufficient pattern fidelity
NO SOLUTION

ArFi – 1D only
6-8 exposures in 3 layers
(use separate layers for
horizontal and vertical connections)

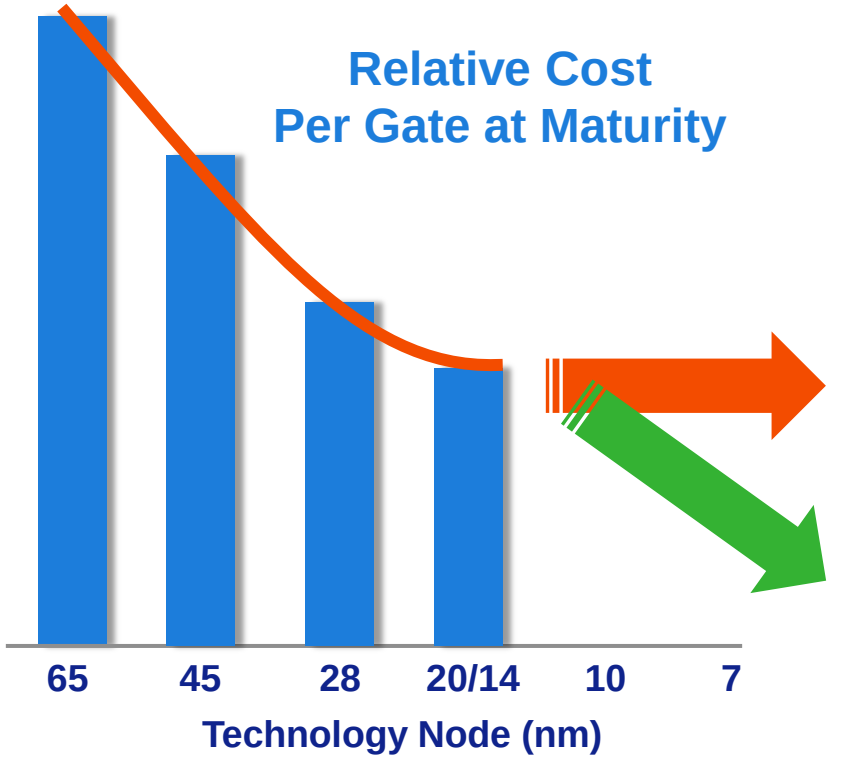


Cost for 2-3 layers > 250%

1-2 extra layers needed
New integration scheme
Significant cost increase

Continued significant cost reduction viewed as possible

but significant innovation is needed

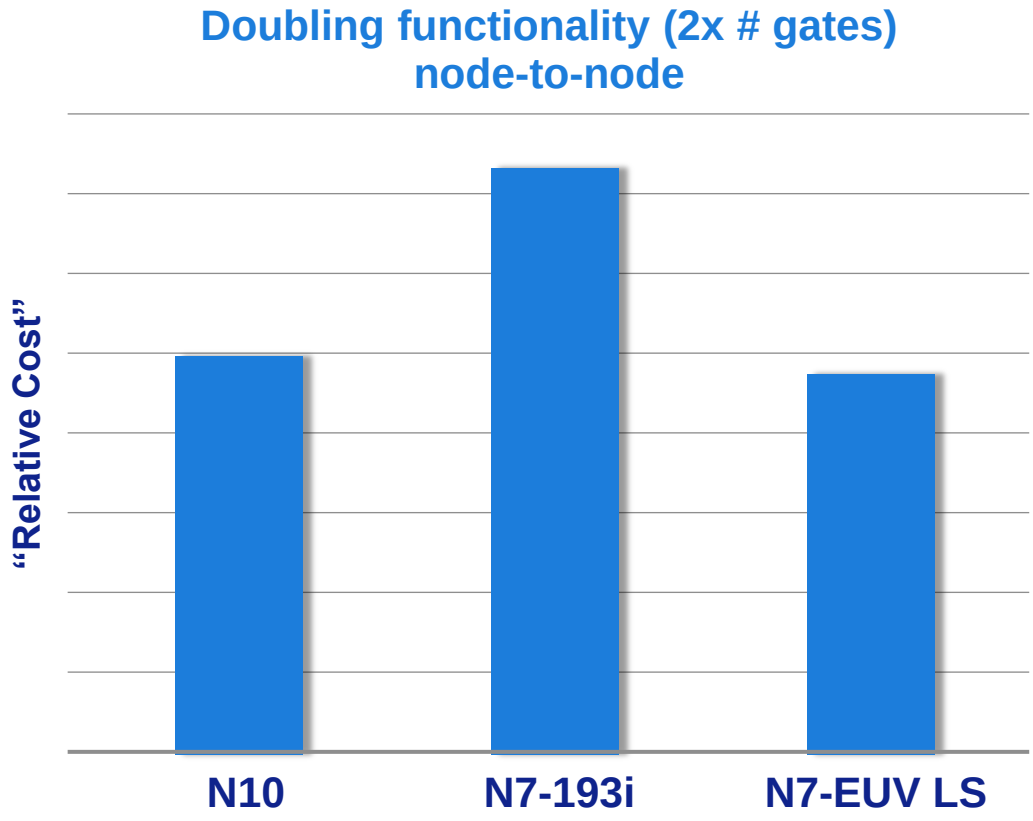


???
"traditional path"
- Primary culprit: litho cost

- New Materials Opportunities
- Multi-pattern cost down
- EUV lithography
- Design/tech co-optimization
- ….

Source: Esin Terzioglu, Qualcomm, EUV symposium, Oct 2014

EUV supports “free functionality” for the 7nm node



Source: Esin Terzioglu, Qualcomm, EUV symposium, Oct 2014

Industry production roadmap summary

ASML

	NAND / Non Volatile Equivalent Node (Feq) Node = (WL + BL) / 2		DRAM / Volatile Memory Equivalent Node (Feq) HP≥ 79% of Feq		LOGIC Node / Metal-HP [nm]	MPU Node / Metal-HP [nm]
2009	35		52		40 / 70	32 / 60 (planar)
2010	28		48		32 / 50	
2011	22		38		28 / 45	22 / 40 (finFET)
2012	19 x 22		33			
2013	19		28 ($6F^2$)		20 / 32 (planar)	14 / 30 (finFET)
2014	16	5x 3D^{24lyrs}	25 ($6F^2$)		14~16 / 32 (finFET)	
2015	16	5x 3D^{32lyrs}	22 ($6F^2$)			10 / 19 (finFET)
2016	13	5x 3D^{48lyrs}	19 ($6F^2$)		10 / 24 (finFET)	
2017	13	5x 3D^{64lyrs}				7 / 12 (finFET)
2018	10	5x 3D^{96lyrs}	16 ($6F^2$)	19 MRAM	7 / 16 (finFET)	
2019	16 ReRAM^{8lrs}	5x 3D^{128lyrs}				5 / 8 (finFET)
2020	12 ReRAM^{8lyrs}	5x 3D^{128lyrs}	16 STT-MRAM		5 / 11 (finFET)	
2021	12 ReRAM^{8lyrs}					3 / 5 (finFET)
2022	10 ReRAM^{8lyrs}		14 STT-MRAM		3 / 7 (finFET)	
	Single expose Pattern split / Cut mask		Double patterning - SPT		Double patterning - LxLE	EUV

Note: Node represents start volume (>10% unit share) of the typical customer roadmap

* Q1-2014 customer roadmaps

Industry production roadmap summary

	NAND / Non Volatile Equivalent Node (Feq) Node = (WL + BL) / 2	DRAM / Volatile Memory Equivalent Node (Feq) HP≥ 79% of Feq	LOGIC Node / Metal-HP [nm]	MPU Node / Metal-HP [nm]
2009	35	52	40 / 70	32 / 60 (planar)
2010	28	48	32 / 50	
2011	22	38		22 / 40 (finFET)
2012	19 x 22			
2013	19			
2014				
2015				
2016			10 / 24 (finFET)	
2017				7 / 12 (finFET)
2018	10 / 5x 3D 96lyrs	16 (6F²) / 19 MRAM	7 / 16 (finFET)	
2019	16 ReRAM 8lrs / 5x 3D 128lyrs			5 / 8 (finFET)
2020	12 ReRAM 8lyrs / 5x 3D 128lyrs	16 STT-MRAM	5 / 11 (finFET)	
2021	12 ReRAM 8lyrs			3 / 5 (finFET)
2022	10 ReRAM 8lyrs	14 STT-MRAM	3 / 7 (finFET)	
	Single expose Pattern split / Cut mask	Double patterning - SPT	Double patterning - LxLE	EUV

Estimated NAND EUV insertion

Estimated DRAM EUV insertion

Estimated Logic EUV insertion

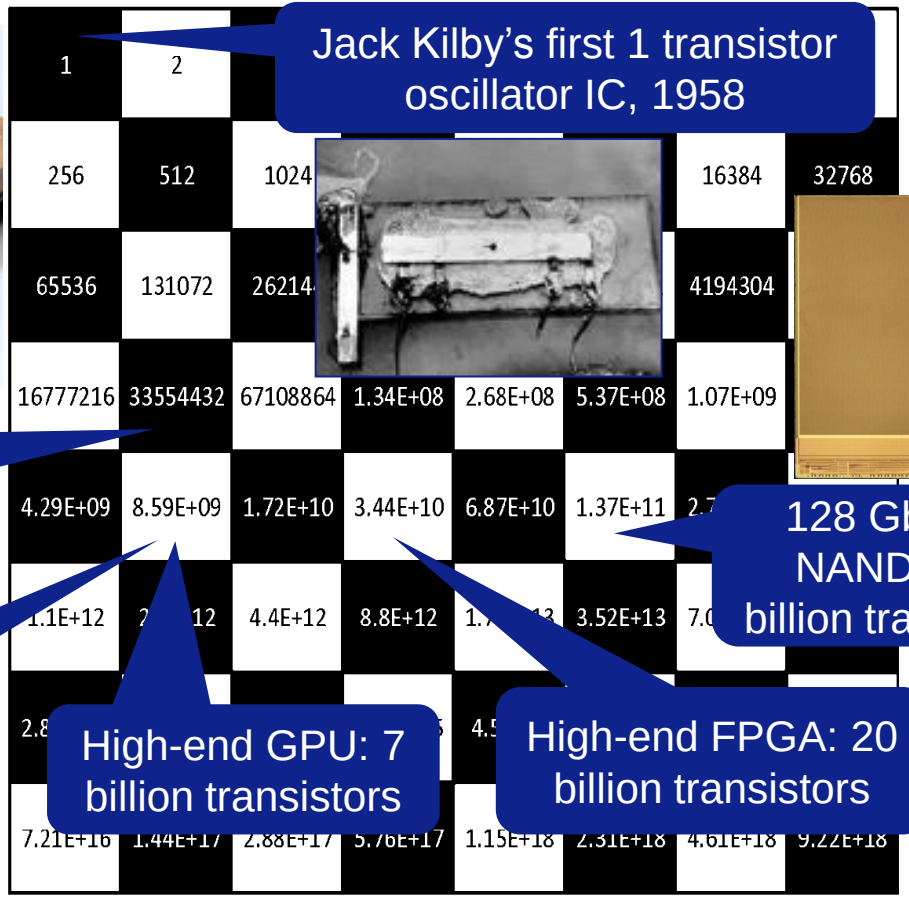
Estimated MPU EUV insertion

Note: Node represents start volume (>10% unit share) of the typical customer roadmap

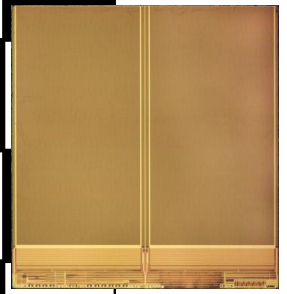
* Q1-2014 customer roadmaps

Our customers moved to the second half of the board

During the past 66 years 1.4 shrink/year, with more moves to come!



Jack Kilby's first 1 transistor oscillator IC, 1958



High-end MPU: 5 billion transistors

6 Gb DRAM: 6 billion transistors

128 Gb SLC NAND: 137 billion transistors

High-end GPU: 7 billion transistors

High-end FPGA: 20 billion transistors

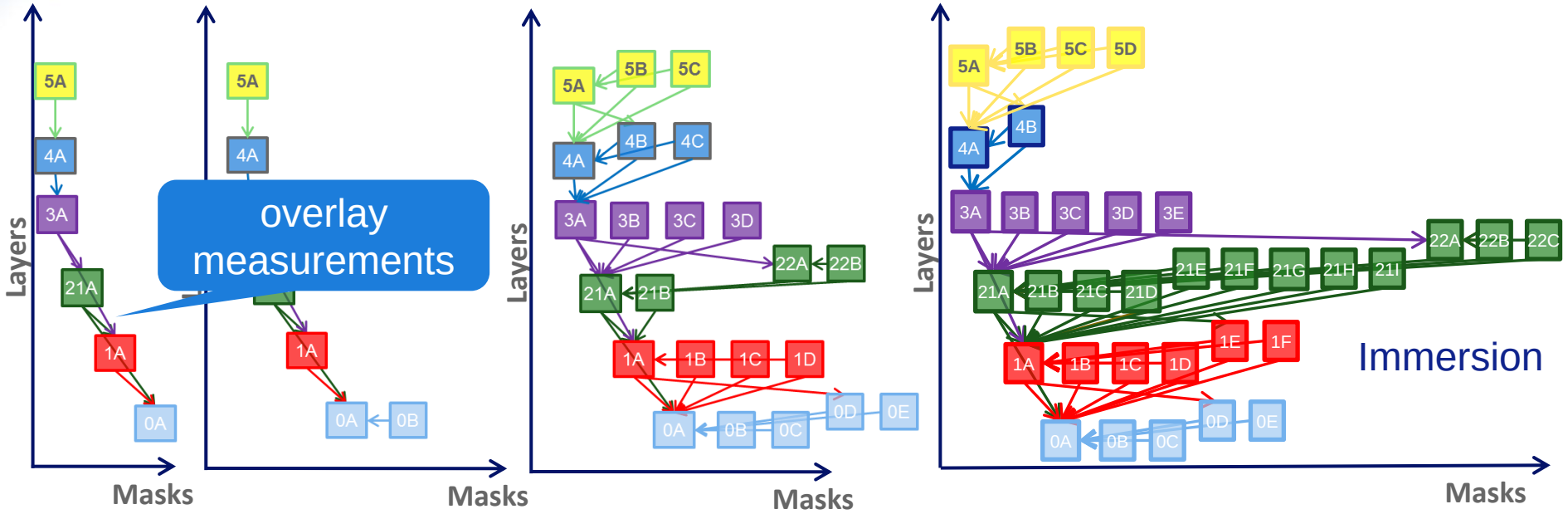
Customer roadmap summary

- Significant innovation ahead in logic including scaling enabling the continuation of cost reduction for the next 10 years
- Logics environment very competitive relative to manufacturing cost dominated by shrink capability
- Memory roadmap to be diversified through the offering on multiple hardware innovations connected through software
- Continued shrink planned for the next 10 years to drive memory cost delivering power and speed performance in the memory architecture
- EUV to bring process simplicity allowing 2D layout enabling more effective shrink

Content

- Industry Challenges
  - The desire to shrink
  - The device challenges
  - The scaling challenges
- ASML Solutions
  - Our holistic approach to extend immersion
  - The process simplification by using EUV

Multi-patterning complexity explodes using immersion



Node	28nm	20nm	10nm	7 nm all immersion
# of lithography steps	6	8	23	34
# OVL metrology	7	9-11	36-40	59-65

Our Challenge: keep scaling affordable

- Scaling needs to create **lower cost and improved performance**
- Affordable scaling in lithography can be achieved:
  - **Holistic Lithography** with both EUV and Immersion to drive **on product** requirements
  - **Immersion**: drive **productivity and yield (overlay and focus control)** with multiple patterning using advanced litho equipment
  - **EUV:** drive **productivity** and improve **operational cost**

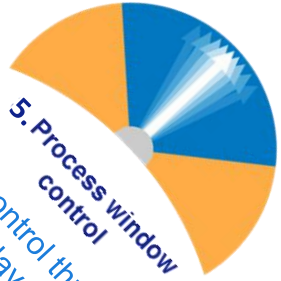
ASML holistic lithography roadmap

Linking the scanner to YieldStar metrology and Tachyon design context

4. Process window enlargement

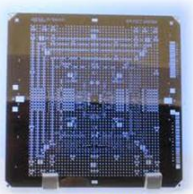
Stepper set up and layout optimization for maximum process window

1. Advanced lithography capability
(Imaging, overlay and focus)



5. Process window control

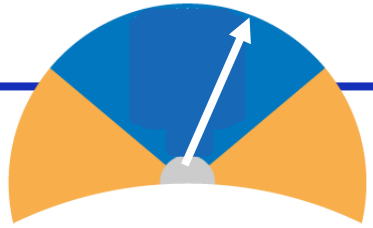
Stepper control through on-product overlay, focus and CD feedback loops window



Product reticles

3. BRION Computational lithography

Design context used to identify hotspot and correct them



6. Process window detection

Product wafers

2. Metrology and control SW

1) TWINSCAN immersion product roadmap

Enabling extension of customer roadmaps and control capital efficiency

Application Node Logic	Application Node DRAM	190 WpH	230 WpH	250 WpH	>275 WpH	On product overlay	1st Shipment
28	2H	NXT:1950i				7 nm	2009
	2M		NXT:1960Bi			6.5 nm	2011
			SNEP 1	NXT:1965Ci	PEP 275	6.5 nm	2013
20/16/14	2L			NXT:1970Ci	PEP 275	<5 nm	2013
				SNEP 2			
10	1H				NXT:1980Di	<3.5 nm	2015
7	1M				NXT:next	2.5 nm	2017

SNEP: System Node Extension Package

PEP: Productivity Enhancement Package

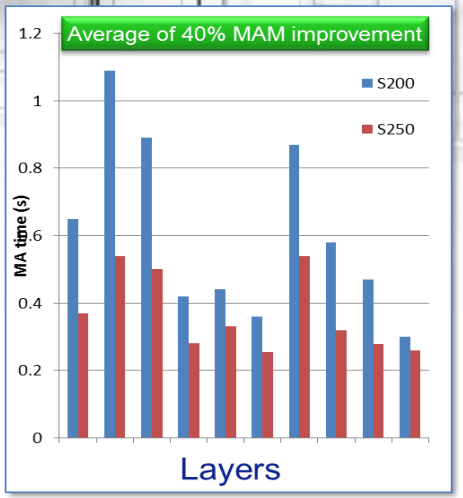
2) YieldStar 250D; latest ASML metrology system

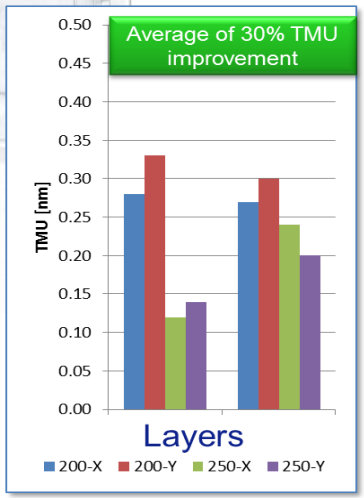
Providing Overlay, Focus and CD feedback for scanner control

Illumination
- Laser Pumped Plasma Source
- Narrow and wideband filters
- Wavelength extension to 765nm

Sensor:
- Optics to support wavelengths up to 780nm
- Faster cameras with higher detection efficiency

S-250D

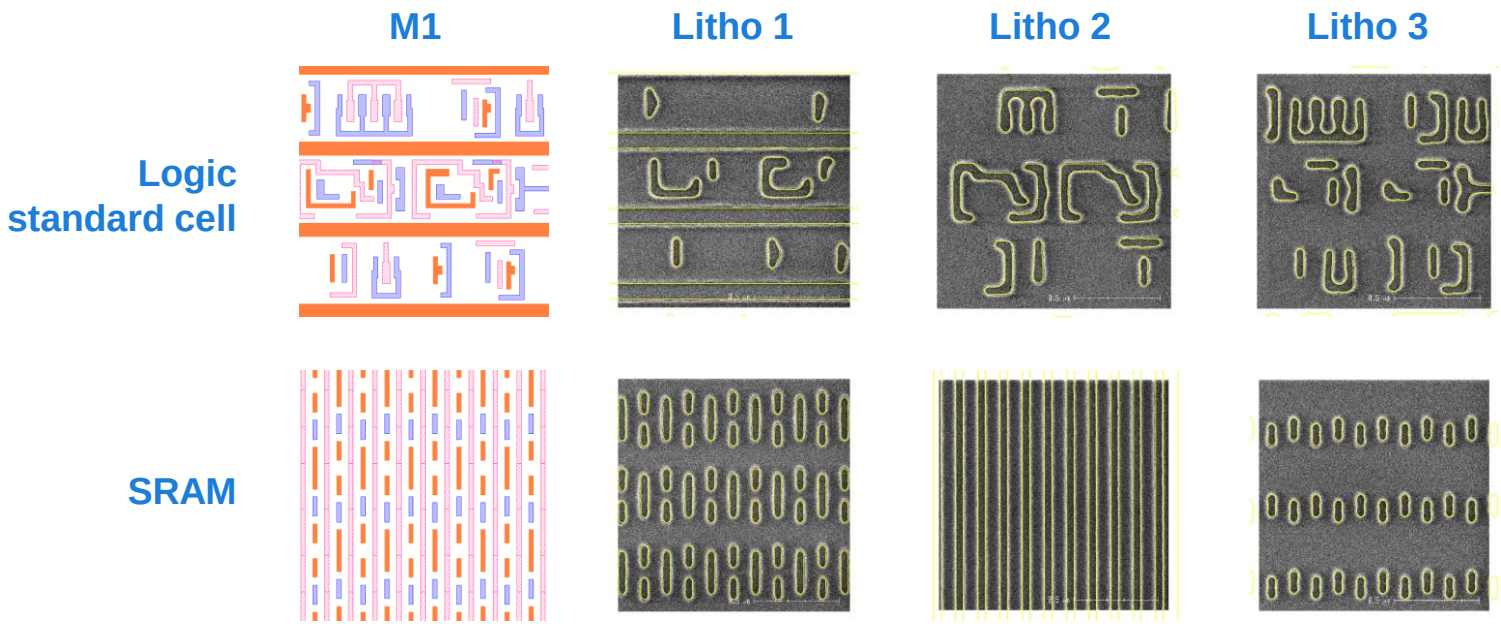




3) Negative tone develop model validation

10nm node metal layer wafer results (triple patterning, LELELE)

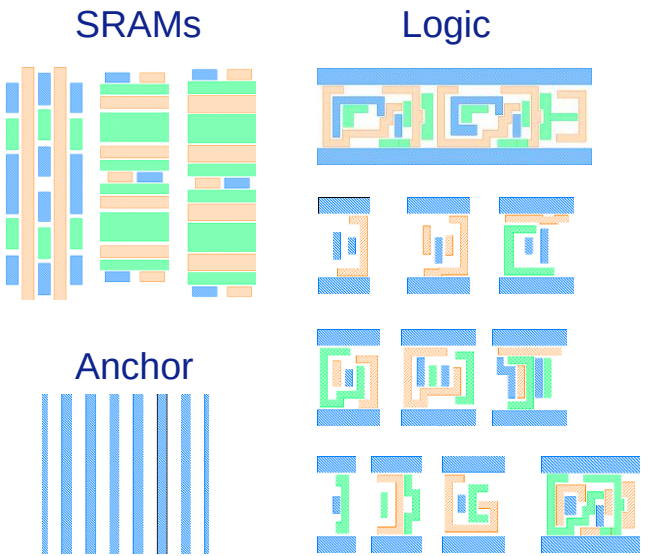
Model calibration RMS: 2nm (1D & 2D), Wafer DOF: 80nm, Across wafer CDU: 1.1nm

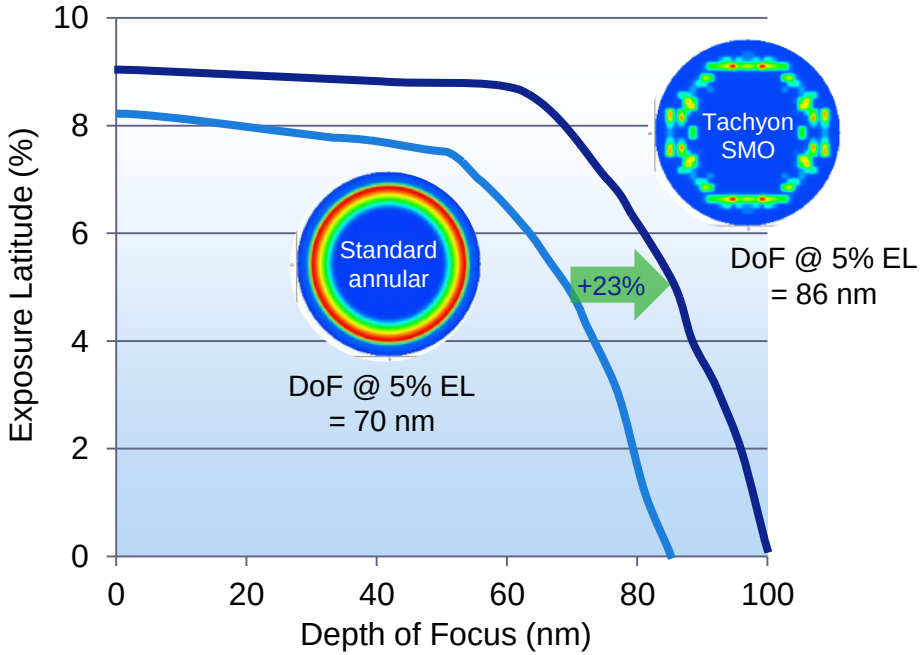


Source: Imec

4) Source-mask optimization of flexible illumination

improves triple patterning process window >23%



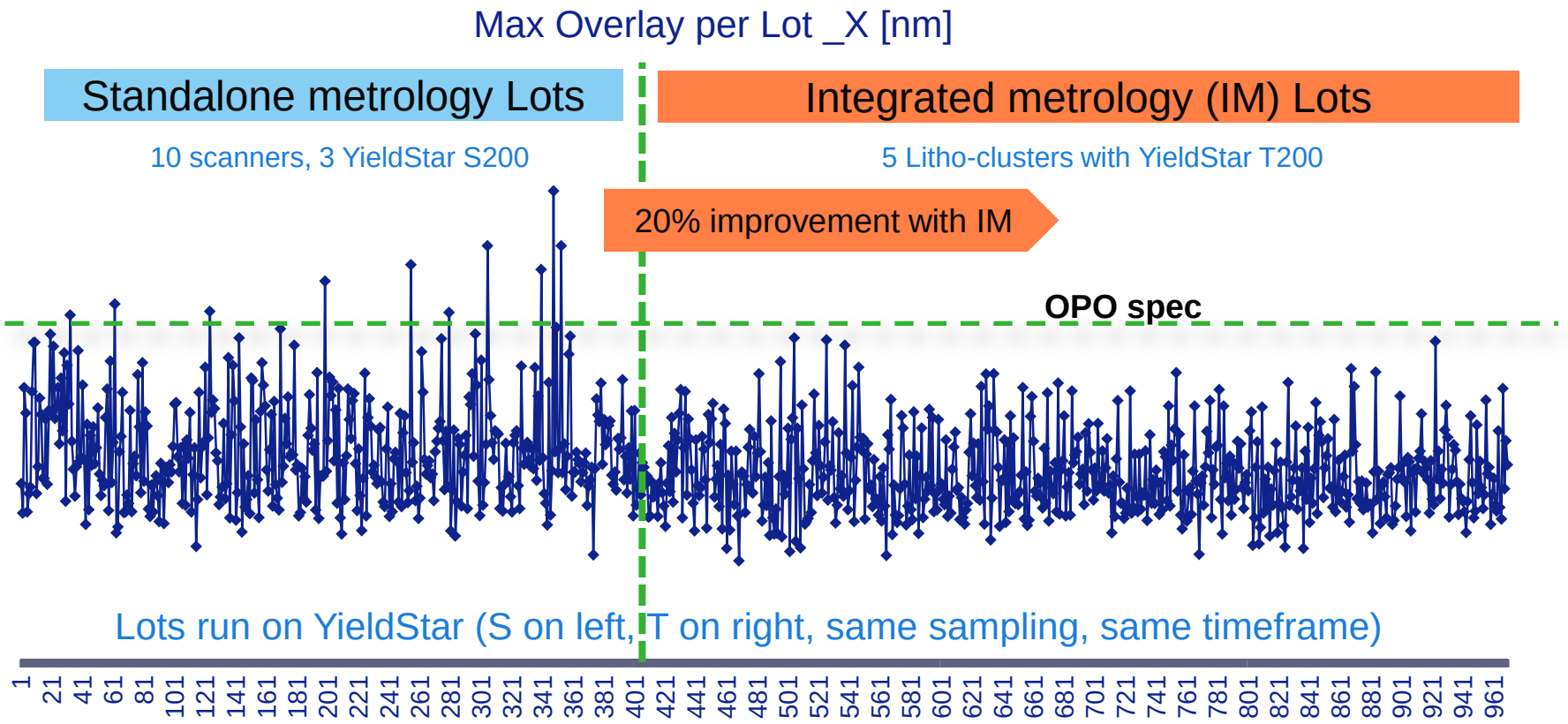


- 10nm node metal1: 48nm min. pitch, 3 splits, NTD and M3D models used
- One common source optimized for best imaging of all 3 splits (LELELE)

Source: Imec

5) 20% improvement in On Product Overlay (per lot)

looking at the biggest excursions using integrated metrology



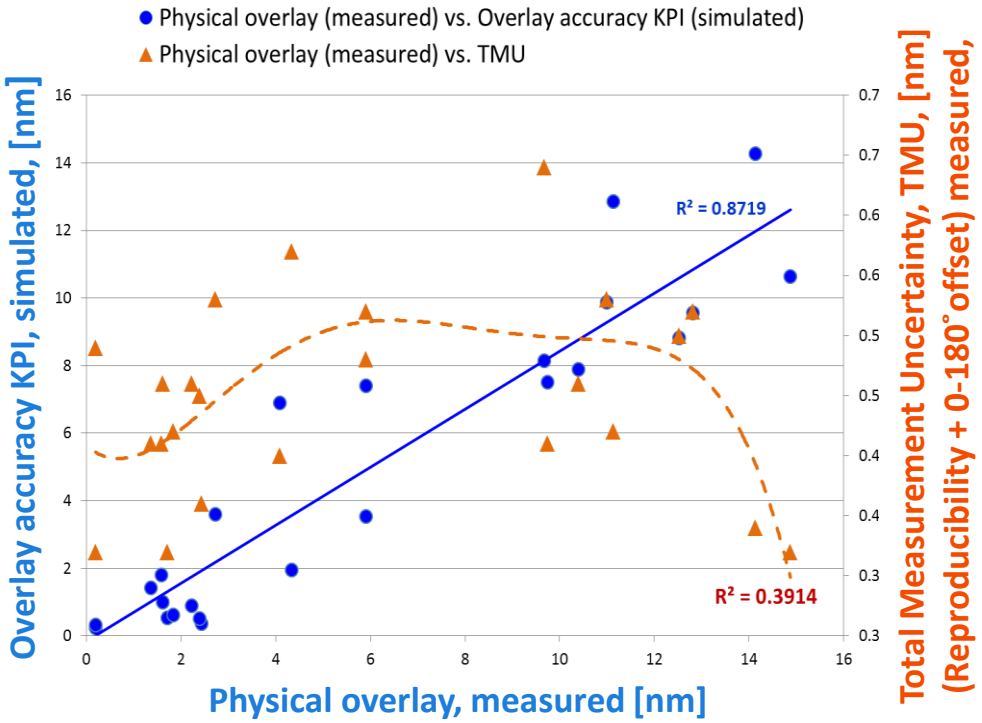
One month production data 2x node BEOL layer

Each data point is one Lot

6) Computational lithography now enters the fab

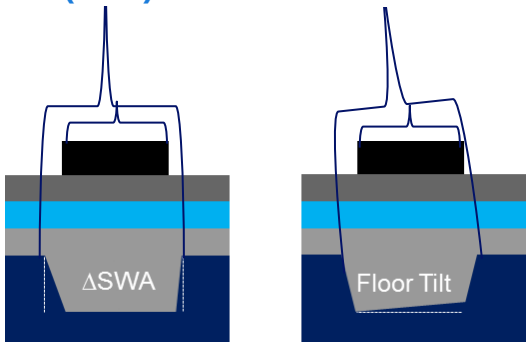
provide metrology context reducing target and recipe design qualification

Overlay simulated and measured on customer product wafers of various markers and recipe combinations



Physical overlay measurement (SEM)

Overlay accuracy KPI Simulated



Overlay (Accuracy) KPI: $\frac{\partial OVL}{\partial Asymi}$

$Asym_i = \{\Delta SWA, \text{Floor tilt}, \ldots\}$

MIN
Marker, recipe

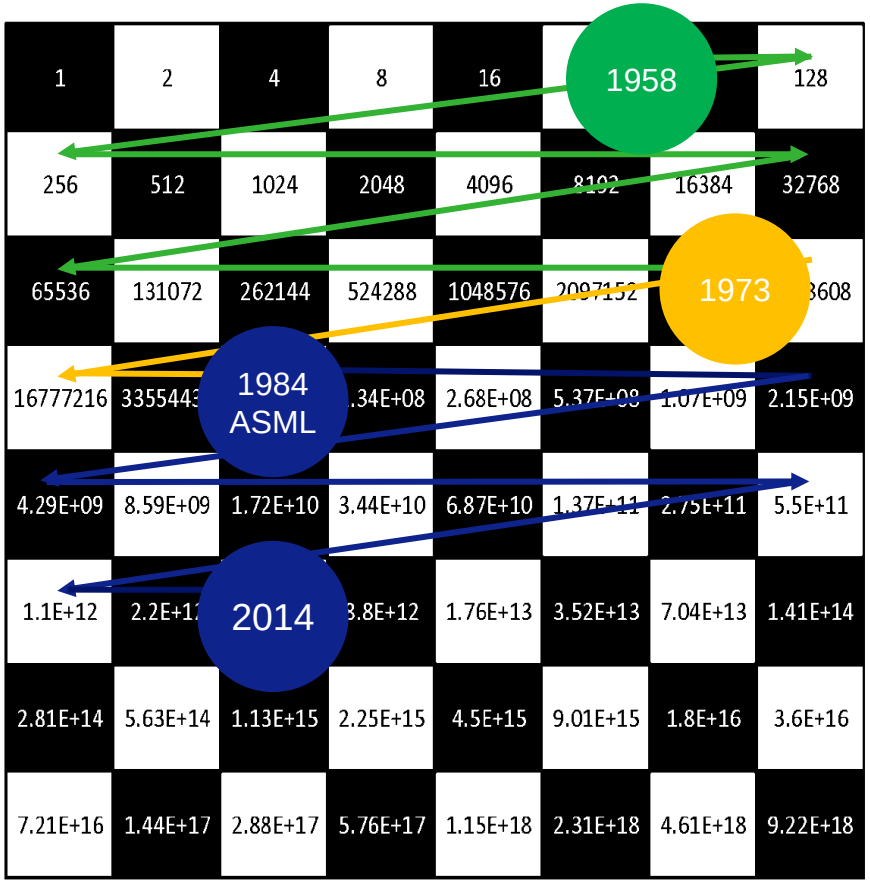
Overlay KPI
(marker, recipe)

ASML enabled 18 moves on the chessboard in 30 years

1973: 1:1 Scanners,
3 um, 75 mm Wafers, 40 Wafers/hr,
5.4 Mpixel/s

1984: G/H line
1,2 um, 100 mm Wafers, 40 W/hr,
61 Mpixel/s

2014: 193 nm Immersion
19 nm, 300 mm Wafers, 250 W/hr,
14 Tpixel/s

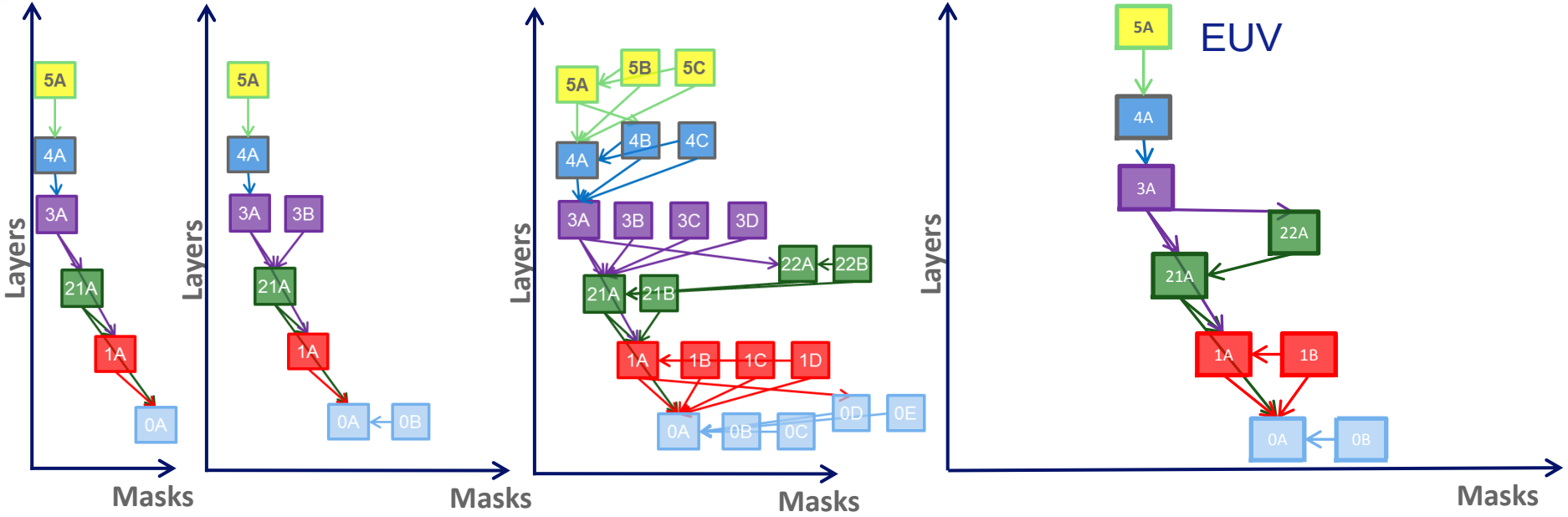


Contact printing

1:1 scanners

DUV step scan or expose and repeat

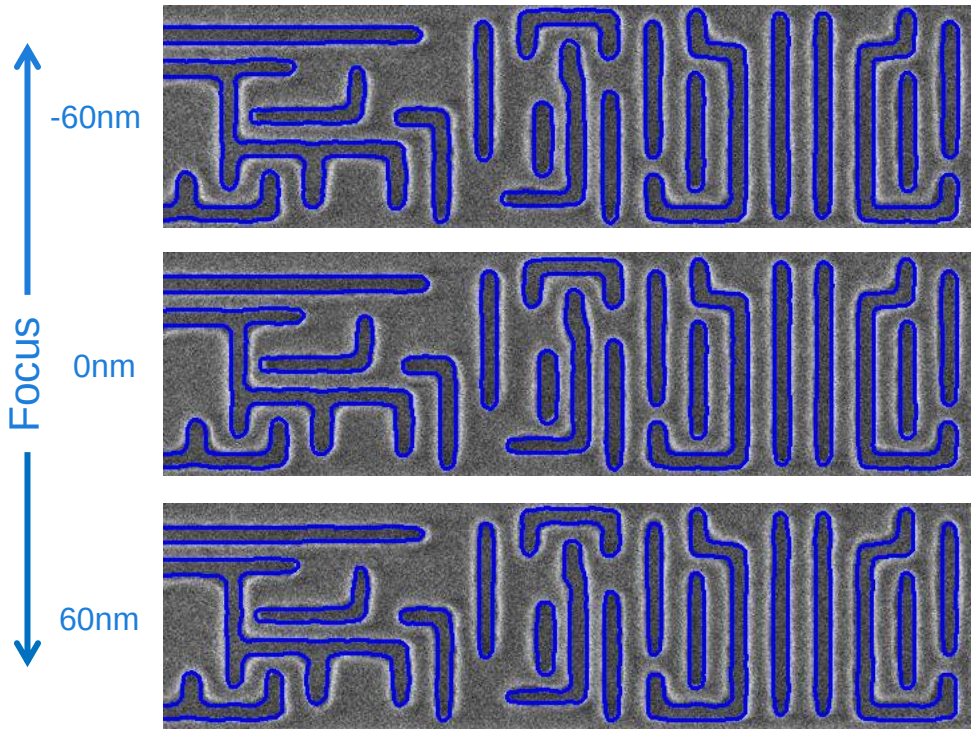
Multi-patterning could explode, but EUV will simplify
through less patterning and metrology steps



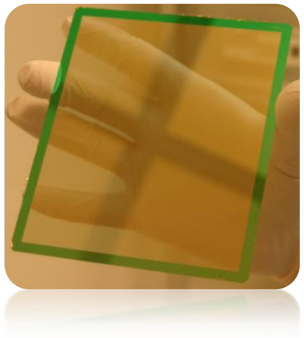
Node	28nm	20nm	10nm	7nm all immersion	7nm all EUV
# of lithography steps	6	8	23	34	9
# OVL metrology	7	9-11	36-40	59-65	12

NXE:3300B litho performance proven

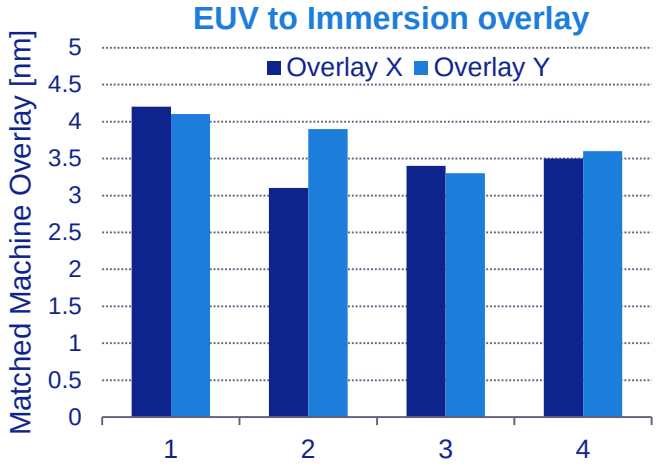
Good imaging, overlay and full field pellicles



NXE:3300B, 10 nm logic metal 1 layer example, 45 nm minimum pitch, 1.6 nm RMS



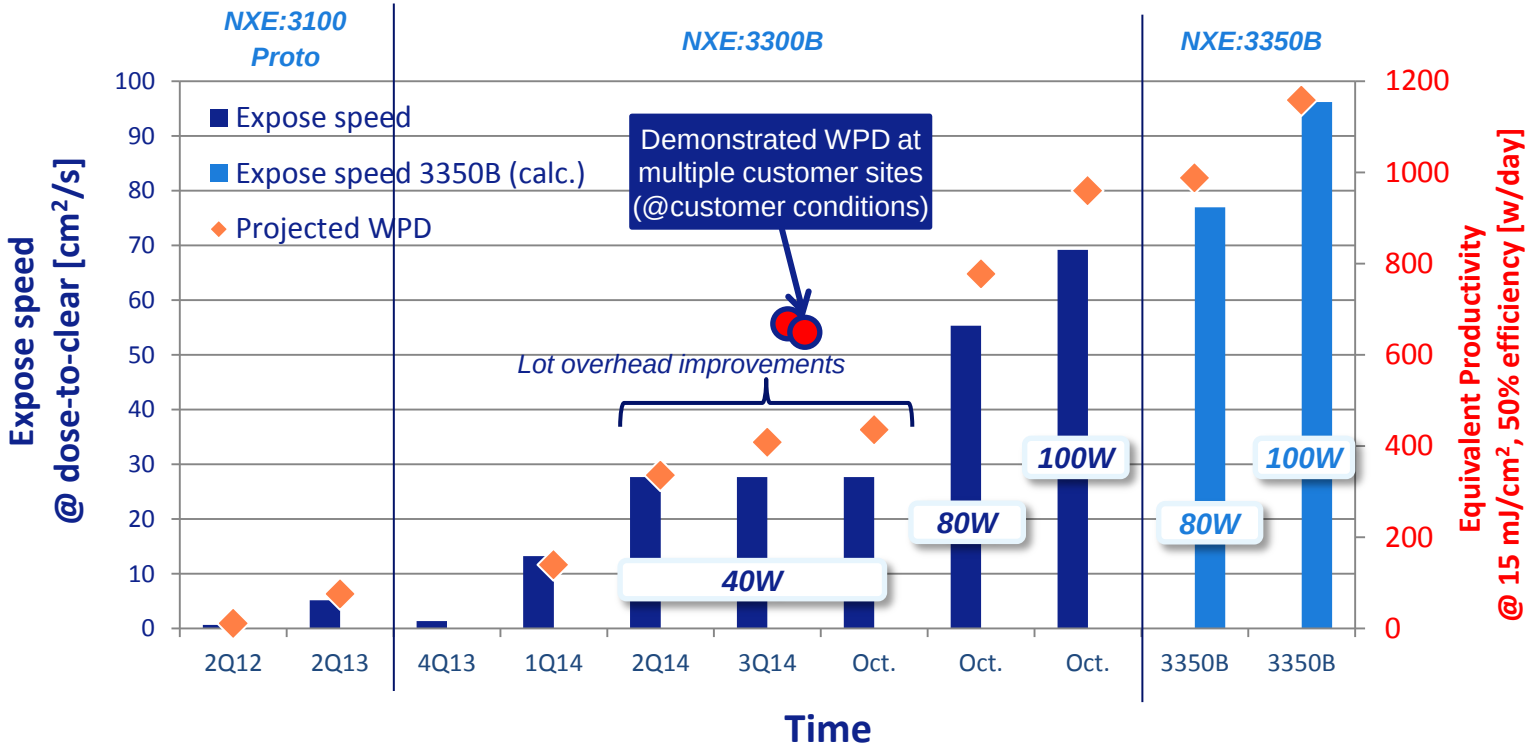
Full size pSi pellicle realized, 103x122 mm, 85% (single pass) transmission mounting an evaluation in progress



Source: ST, 2014

NXE:33x0B demonstrated power supports >1000 wpd

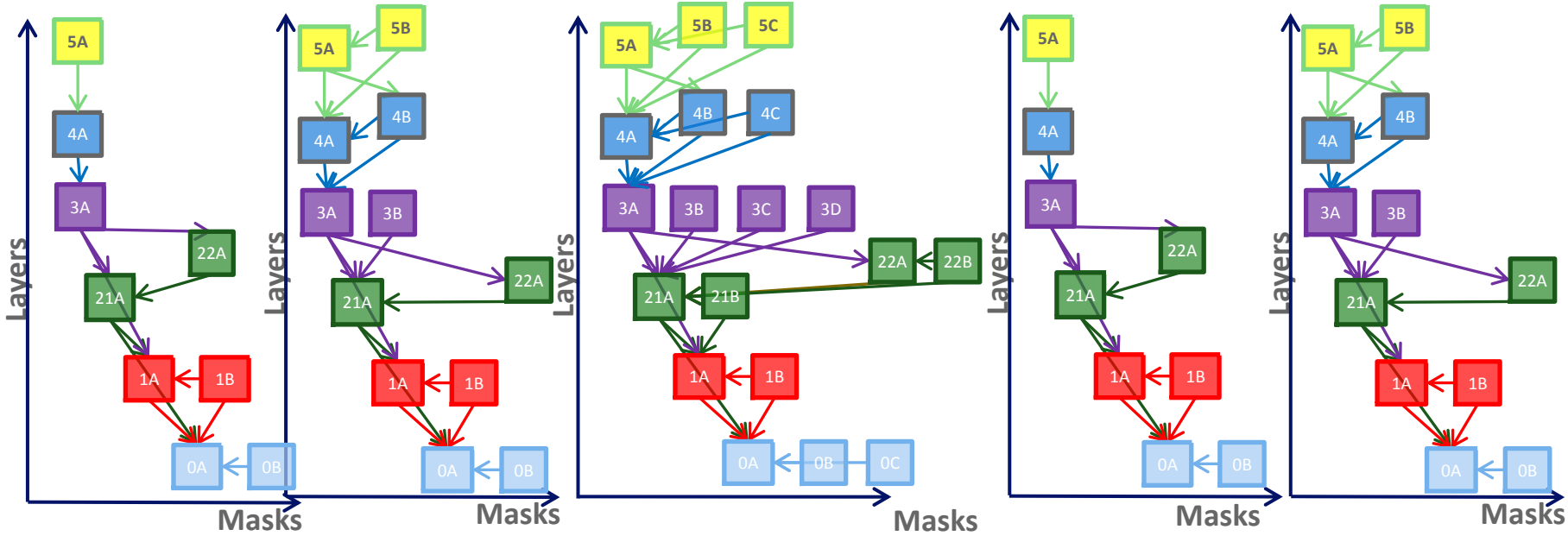
Up to 7 systems operational at >40W; 100W source operation demonstrated



- Dose-to-expose is 2.5x dose-to-clear
- Productivity: field size 26x33 mm², 96 fields/wafer, 50% efficiency
- NXE:3350B data calculated using measured transmission of last system

Multi-patterning planned with EUV on future nodes but…

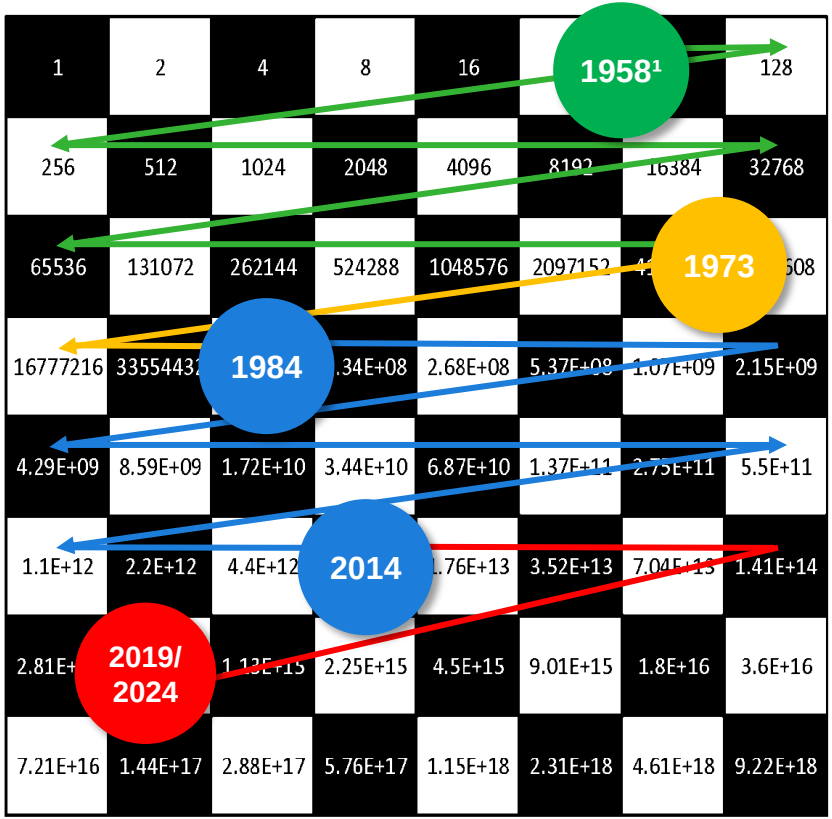
>0.5 high-NA will simplify and extend roadmap again



Node	7nm - EUV	5nm - EUV	3nm - EUV	5nm - high NA EUV	3nm - high NA EUV
# of lithography steps	9	12	19	9	12
# OVL metrology	12	18-22	29-36	12	18-22

We are preparing to make another 6 moves in 10 years

Our next move: 13nm EUV lithography



2019-2024: 13nm EUV
3 nm, 300 mm Wafers,
200 W/hr, 0.45 Ppixel/s

Contact printing

1:1 scanners

DUV step scan or expose and repeat

EUV

[1]Jack Kilby's oscillator contains ~ 50 pixels to be exposed through contact printing in 1 sec

Summary

- Node progression enabled by immersion multi pass patterning and extended litho metrology and computational litho to control complexity
- To address highly complex multi-patterning schemes, EUV insertion is likely at the 10nm logic and 7nm MPU node with full production one node later
- ASML has demonstrated consistent EUV source progress. Today performance approaching 100W exposure power. System uptime remains a key challenge
- EUV infrastructure supportive for above transition scenarios
- Lithography roadmap defined down to the 3nm node

Had the King's name been Moore….

He would have worked to find ways to scale down his grains, keep their nutritional value and double the amount with every move.
He could have fed the world, instead of having lost a Kingdom.

ASML

INVESTOR DAY

ASML SMALL TALK 2014

LONDON